Name: _____

Problem 1 (20%). Given the following **direct-mapped** cache architecture:
All instructions use byte addresses. The address bus is 8 bits. A word size is 16 bits.
Total data cache size 4 words.

1a. (2%) How many bits is the index?

1b. (2%) How many bits is the byte offset?

1c. (2%) How many bits is the tag size?

1d. (14%) For the following instruction sequence, fill in the access bits to the **data cache**

tag	index	byte offset	instruction
			lw $1, 32($0)
			lw $2, 34($0)
			add $3, $1, $2
			sw $3, 44($0)
			lw $4, 12($0)
			lbu $5, 41($0)
			beq $1, $2, 34($0)

Problem 2 (10%). Given the following **2-way set associative** cache architecture:
All instructions use byte addresses. The address bus is 8 bits. A word size is 16 bits.
Total data cache size 4 words.

2a. (2%) How many bits is the index?

2b. (2%) How many bits is the byte offset?

2c. (2%) How many bits is the tag size?

2d. (4%) For the following instruction sequence, fill in the access bits to the **data cache**

tag	index	byte offset	instruction
			lw $1, 32($0)
			lbu $2, 33($0)

Problem 3. (15%) For the following instruction sequence fill in the direct-mapped cache
The word size is 16 bits.
Memory[0]=0x1066; Memory[2]=0x1453; Memory[16]=$3=0x1776; Memory[20]=0x1914;

3a. (5%) Fill in the miss cache column.

tag	index	byte offset	instruction	Valid or Tag Cache Miss?
000	00	0	lw $1, 0($0)	
000	01	0	lw $2, 2($0)	
010	00	0	sw $3, 16($0)	
010	10	1	lbu $5, 21($0)	
010	10	0	lw $6, 20($0)	

3b. (10%) The final state of the direct mapped data cache is:

index	valid	tag	data

Problem 4. (15%) For the following instruction sequence fill in the 2-way set associative LRU cache
The word size is 16 bits.
Memory[0]=0x1066; Memory[2]=0x1453; Memory[16]=$3=0x1776; Memory[20]=0x1914;

4a. (5%) Fill in the miss cache column.

tag	index	byte offset	instruction	Valid or tag Cache Miss?
000	0	0	lw $1, 0($0)	
100	0	0	sw $3, 16($0)	
000	0	1	lbu $5, 1($0)	
101	0	0	lw $6, 20($0)	
000	1	0	lw $1, 2($0)	

4b. (10%) The final state of the 2-way set associative LRU data cache is:

index	valid	tag	data
0			
1			

Problem 5. (10%) Given a 1-word cache entry block size and one word wide memory bus organization (figure 7.13a, page 561), and the following access times:

1 clock cycle to send the address,
8 clock cycles to read access DRAM, 16 clock cycles to write to DRAM
1 clock cycle to to send a word

5a. (5%) What is the miss penalty for a write-through direct mapped cache?

5b. (5%) What is the miss penalty for a write-back direct mapped cache?

Problem 6 (20%). Given the following **virtual memory** architecture:

All instructions use byte addresses. The virtual address bus is 16 bits. A word is 16 bits.
Total page size 8 bytes. The real memory address bus is 16 bits.

6a. (2%) How many bits is the page offset?

6b. (2%) How many bits is the physical page number size?

6c. (2%) How many page table entries?

6d. (2%) How large is the page table?

6e. (12%) For the following instruction sequence, fill in the data access bits to the **page table**

virtual page number	page offset	instruction
		lw $1, 32($0)
		lw $2, 34($0)
		lbu $5, 41($0)

Problem 7. (10%) Assume 2K real memory, LRU, a page size of 1K and no pages loaded.
Fill in the page fault columns

instruction	Page fault?	Flush which page?	Write flushed page to disk?	Load what new page
lw $1, 32($0)				
lw $2, 34($0)				
lbu $5, 41($0)				
sw $6, 1100($0)				
lw $7, 2000($0)				
lw $1, 4100($0)				
lw $2, 32($0)				