EECS 322 **Post** Test 2 (12 points) Due Monday April 2, 2001

Name: _____ Email: _____

Problem 1: A group of EECS students have decided to compete with Motorola Corporation in the embedded DSP wireless network market. The RISCEE3 computer is a **16** bit single-cycle computer.

There is only **1 register** (i.e. accumulator, called A). The PC and alu are eight bits wide.
Note: You can remove and keep the RISCEE3 and RISCEE4 diagrams from the exam.
Remember: anything AND with zero is always zero. Anything OR with one is one.

There is only one instruction format shown as follows:

Opcode	**Data8 or Address8 field**
8 bits	8 bits
15-8	7 - 0

(a) Fill in the settings of the control lines determined by the all the instructions (use X for Don't Care)

Machine Instruction	Operation	RegDst	ALU	MemWrite	RegWrite	BZ	P0
clear	A = 0						
addi data8	A = A + data8						
add addr8	A = A + Memory[addr8]						
store addr8	Memory[addr8] = A						
bne addr8	If (A != 0) { PC = addr8;}						
apc	A = PC+2						

(b) Using the above instruction set, fill in the code for the pseudo-instructions

Pseudo-Instruction	Operation	Assembly machine instructions (from part 1a)
loadi data8	A = data8	
load address8	A = Memory[addr8]	
jmp address8	pc = address8	
jal address8	A=PC+x; PC=addess8 *Where A really contains the return address after the pseudo instruction returns. (Assume PC never becomes zero)*	

Problem 2: The Credit Suisse First Boston investment bank will only invest in the multi-cycle RISCEE4 architecture for the machine instructions of problem 1a. Use X for Don't Care. Assume parts 2a, 2b, 2c are independent of each other. **Do it in the <u>minimum</u> number of clocks.**

(a) Fill in the settings of the control lines needed for the **"clear"** instruction.

Clock Step	Mem Write	Mem Read	IorD	IR write	P0	BZ	PC src	ALU op	ALU srcA	ALU srcB	Reg Write	Reg Dst
T_1												
T_2												
T_3												
T_4												
T_5												

(b) Fill in the settings of the control lines needed for **"add"** *from memory* instruction.

Clock Step	Mem Write	Mem Read	IorD	IR write	P0	BZ	PC src	ALU op	ALU srcA	ALU srcB	Reg Write	Reg Dst
T_1												
T_2												
T_3												
T_4												
T_5												
T_6												

(c) Fill in the settings of the control lines needed for **"bne"** instruction

Clock Step	Mem Write	Mem Read	IorD	IR write	P0	BZ	PC src	ALU op	ALU srcA	ALU srcB	Reg Write	Reg Dst
T_1												
T_2												
T_3												
T_4												
T_5												
T_6												

Problem 3. Look up the the following patent

- US Patent 5153921 Microcomputer, 1992

  using **http://www.delphion.com** with the search word as the patent number.
  Note: use the View Images for the first free 7 pages

Check the web for patent infringement. For example, **http://www.intellectual.com/patinfr.htm** or use **http://www.google.com**

(a) Briefly explain what claims (and sub items within a claim) match & don't match the RISCEE 3 architecture? Does RISCEE3 infringe on their patent?

(b) Briefly explain what claims (and sub items within a claim) match & don't match the RISCEE 4 architecture? Does RISCEE4 infringe on their patent?