EECS 322 Sample Test 2 Wednesday March 21, 2001

Name: _____

Problem 1 (50%): A group of EECS students have decided to compete with Intel Corporation in the microcontroller market. Their first prototype called the RISCEE1 computer is a 16 bit single-cycle computer build in a secret lab in Olin building.
The all 16 registers, pc, and alu are eight bits wide. Register zero (r0) contains only a zero and cannot be overwritten. There is only one instruction format shown as follows:

Opcode 4 bits 15-12	Register 4 bits 11-8	Data or Address field 8 bits 7 - 0

The delay time of the functional units are as follows Memory Write 5 ns, Memory Read 3 ns, Register (read or write) 2 ns, and ALU & Adders 2 ns.

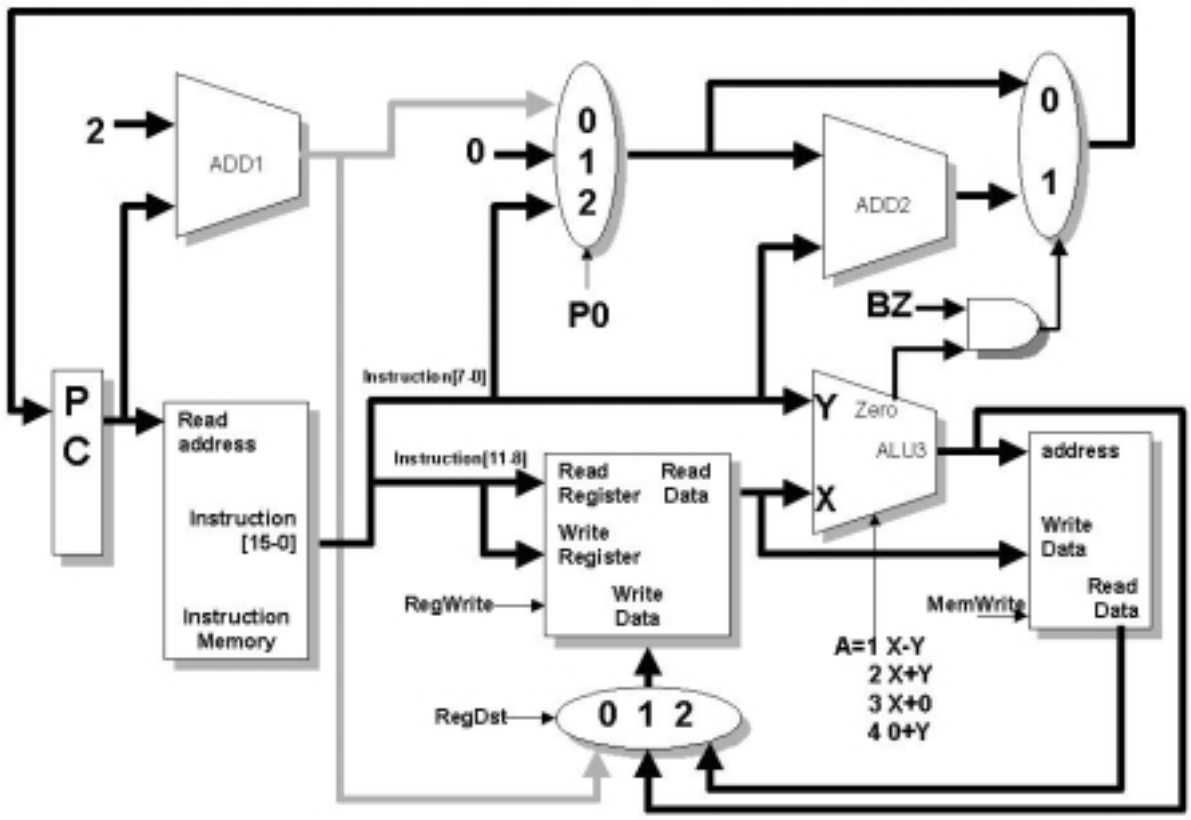
(a) Fill in the settings of the control lines determined by the all the instructions (use X for Don't Care)

Instruction	Operation	RegDst	A	MemWrite	RegWrite	BZ	P0
addi reg, data8	reg = reg + data8						
subi reg, data8	reg = reg – data8						
load reg, address8	reg=Memory[address8]						
store reg, address8	Memory[address8]=reg						
beq reg,address8	If (reg==0) { pc=pc+address8; }						
jmp address8	pc = address8						
jal reg, address8	reg=pc+2;pc=address8						

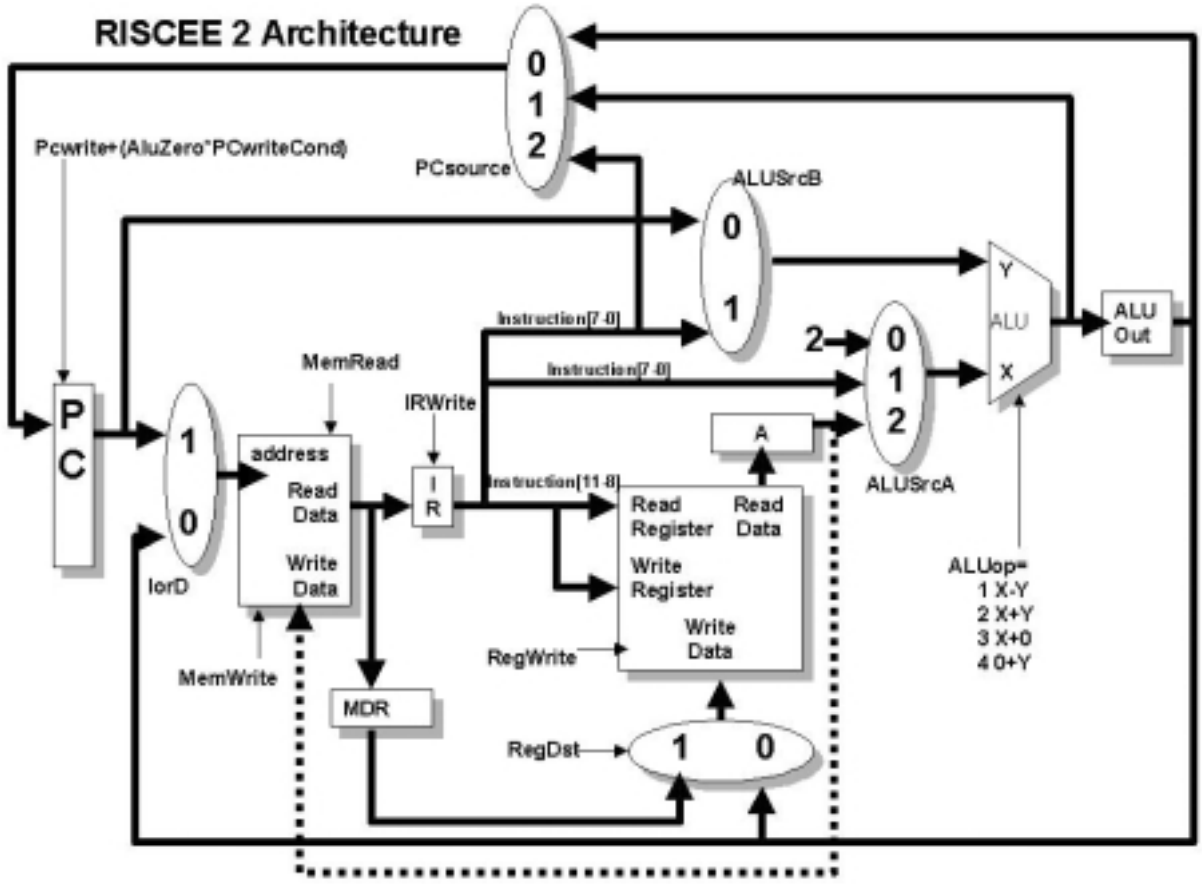
(b) Write"fail" for instructions will stuck-at-fault for RegDst

Instruction	RegDst Stuck-at-0	RegDst Stuck-at-1
addi		
subi		
load		
store		
beq		
jmp		
jal		

RISCEE 1 Architecture



RISCEE 2 Architecture



(c) Fill in critical path times for each instruction.

Instruction	Instruction memory	Register Read	ALU operation	Data Memory	Register Write	Total Time	Clock Cycles	Instruction Mix
addi								40%
subi								0%
load								25%
store								10%
beq								25%
jmp								0%
jal								0%
						Clock Speed		
						CPI		
						MIPS		

(d) Fill in the Clock, CPI, and MIPS in the above table and show all calculations (Hint, single-cycle computer).

(e) Using the RISCEE1 instruction set, show how to swap two registers r1 and r2 (hint, use memory).

Problem 2 (50%): The brokerage firm said they talked to their investors and said they will only invest in multi-cycle computers. Furthermore, CPU Benchmarks showed that the subi, jmp, and jal instructions are not used.

(a) Draw the finite state machine for multi-cycle RISCEE 2 architecture (addi, load, store, beq), show all states.

(b) Place next to each state the amount of time needed to process that state.

(c) Fill in critical path times for each instruction (copy delay times from part b).

Instruction	Instruction memory	Register Read	ALU operation	Data Memory	Register Write	Total Time	Clock Cycles
addi							
load							
store							
beq							

(d) Determine the fastest clock speed for the computer to work properly in frequency and show why.

(e) Fill in the Clock, CPI, and MIPS in the above table and show all calculations.

Instruction	Clock Cycles	Instruction Mix
addi		40%
load		25%
store		10%
beq		25%
Clock speed		
CPI		
MIPS		

(f) Suppose you do not know the instruction mix. Explain which one functional unit (Memory write 5ns, Memory Read 3ns, Register 2ns, or ALU 2ns) would you choose to improve by 1 ns and what will be the new clock speed? (show calculations)

Extra Credit which can be only used for this exam and the previous exam.

a) (9%). Assemble the following machine instructions into binary,

Assume each instruction is located at address **0x45891280**

Field 1	Fields 2 and etc	instruction
		`j 0x458912A0`
		`beq $s1,$t4,0x45891380`
		`jal 0x45891388`

b) (2%) Give the two's complement of the 8 bit binary 0x12

c) (2%) Convert –25 into a 8 bit binary.

d) (2%)Convert the 5 bit signed binary 10010 into decimal

e) (5%) Add 0x2 and 0xF and what is the **overflow bit =** _____

Cin				
Sum				
Cout				

f) (5%) Multiply the 3 bit signed numbers 010 by 110 into a 6 bit signed number.