

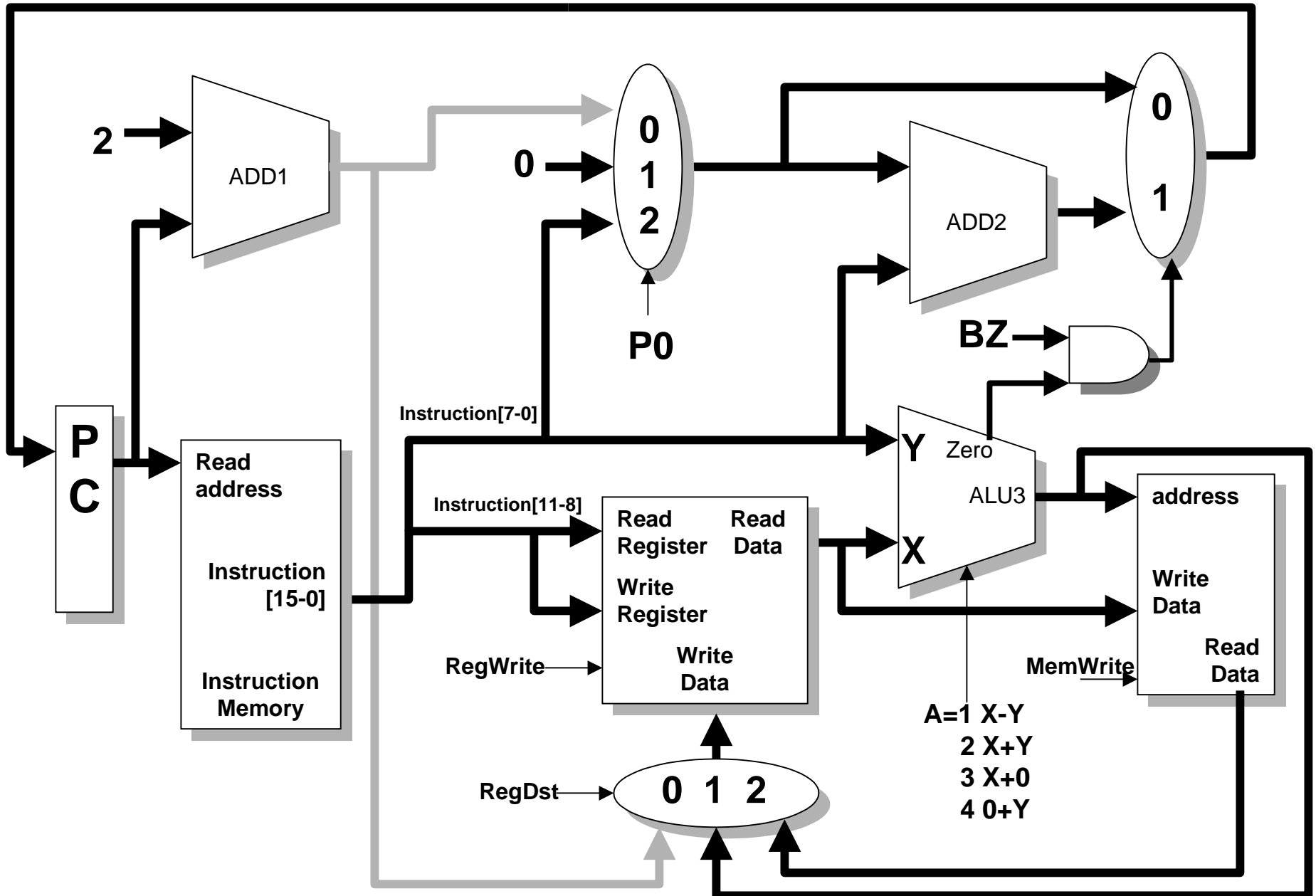
**Problem 1 (50%):** A group of EECS students have decided to compete with Intel Corporation in the microcontroller market. Their first prototype called the RISCEE1 computer is a 16 bit single-cycle computer build in a secret lab in Olin building.

The all 16 registers, pc, and alu are eight bits wide. Register zero (r0) contains only a zero and cannot be overwritten. There is only one instruction format shown as follows:

<b>Opcode</b> 4 bits 15-12	<b>Register</b> 4 bits 11-8	<b>Data or Address field</b> 8 bits 7-0
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The delay time of the functional units are as follows Memory Write 5 ns, Memory Read 3 ns, Register (read or write) 2 ns, and ALU & Adders 2 ns.

# RISCEE 1 Architecture



(a, 10%) Fill in the settings of the control lines determined by the all the instructions (use X for Don't Care)

Instruction	Operation	RegDst	A	MemWrite	RegWrite	BZ	P0
addi reg, data8	reg = reg + data8	1	2	0	1	0	0
subi reg, data8	reg = reg - data8	1	1	0	1	0	0
load reg, address8	reg = Memory[address8]	2	4	0	1	0	0
store reg, address8	Memory[address8]=reg	X	4	1	0	0	0
beq reg, address8	if(reg==0) {pc=pc+2+address8}	X	3	0	0	1	0
jmp address8	pc=address8	X	X	0	0	0	2
jal reg, address8	reg=pc+2; pc=address8	0	X	0	1	0	2

(b, 10%) Write "fail" for instructions that will stuck-at-fault for RegDst

Instruction	Stuck-at-0	Stuck-at-1
addi reg, data8	fail	
subi reg, data8	fail	
load reg, address8	fail	fail
store reg, address8		
beq reg, address8		
jmp address8		
jal reg, address8		fail

(c, 10%) Fill in the critical path times for each instruction

Instruction	Instruction memory	Register Read	ALU operation	Data Memory	Register Write	Total Time	Clock Cycles
addi	3 ns	2 ns	2 ns		2 ns	9 ns	1
subi	3 ns	2 ns	2 ns		2 ns	9 ns	1
load	3 ns		2 ns	3 ns	2 ns	10 ns	1
store	3 ns	2 ns	2 ns	5 ns		12 ns	1
beq	3 ns	2 ns	2 ns			7 ns	1
jmp	3 ns					3 ns	1
jal	3 ns				2 ns	5 ns	1

(d, 10%) Fill in the Clock, CPI, and MIPS in the above table and show all calculations (Hint, single-cycle computer).

<b>Clock speed</b>	83.3 Mhz	= $1/12\text{ns}=83.3\text{ Mhs}$ <b>Clock speed is the slowest instruction</b>
<b>CPI</b>	1	= $1*0.40+1*0.0+1*0.25+1*0.10+1*0.25+1*0+1*0$
<b>MIPS</b>	83.3 MIPS	= $83.3\text{ Mhz}/1$

(e, 10%) Using the RISCEE1 instruction set, show how to swap two registers r1 and r2 (hint, use memory).

Pick any 2 memory addresses, say, 100 and 102

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store    r1, 100
store    r2, 102
load     r1, 102
load     r2, 100
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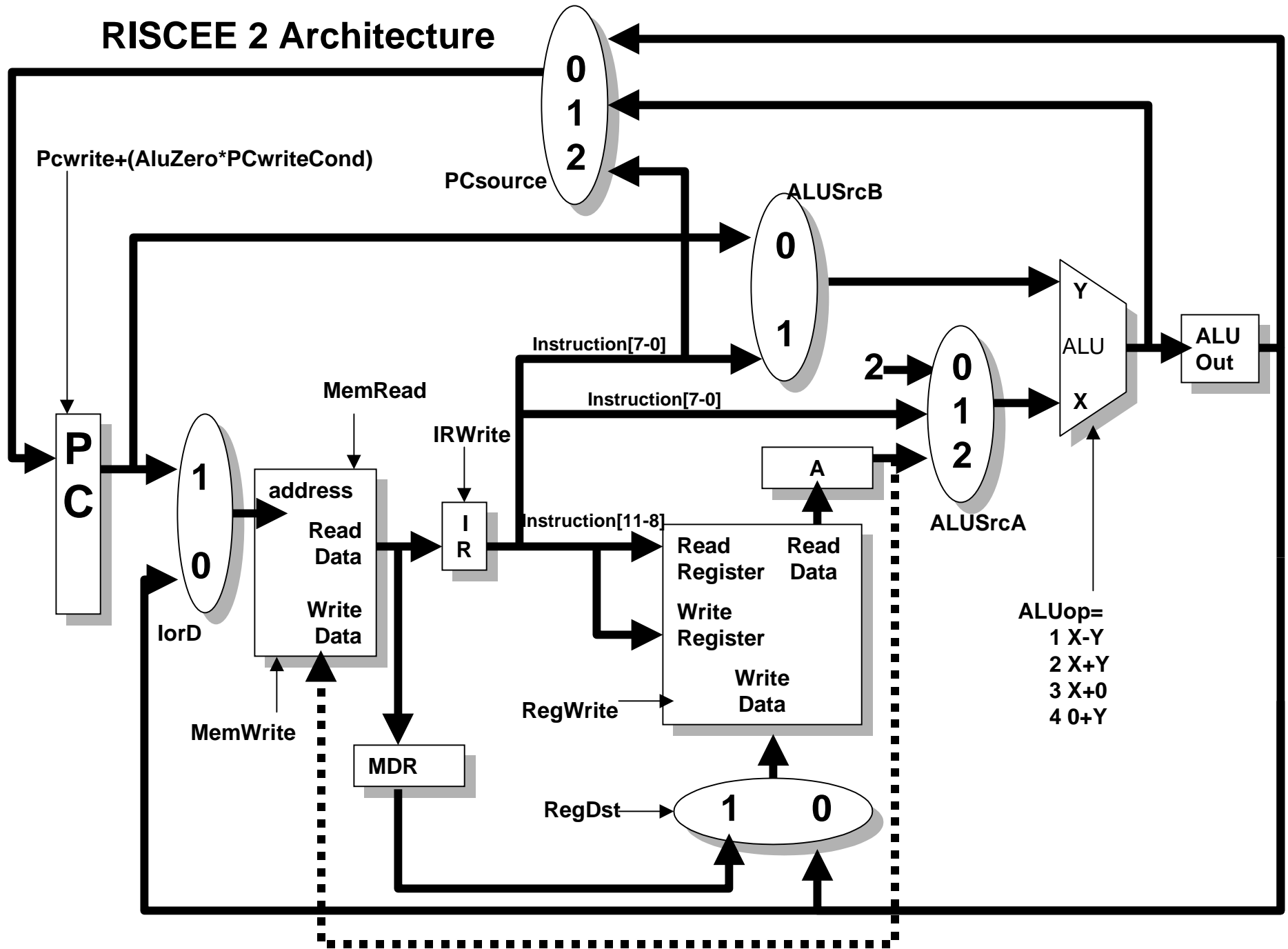
**Problem 2 (50%):** The brokerage firm said they talked to their investors and said they will only invest in multi-cycle computers . Furthermore, CPU Benchmarks showed that the subi, jmp, and jal instructions are not used. The multi-cycle version is called RISCEE 2.

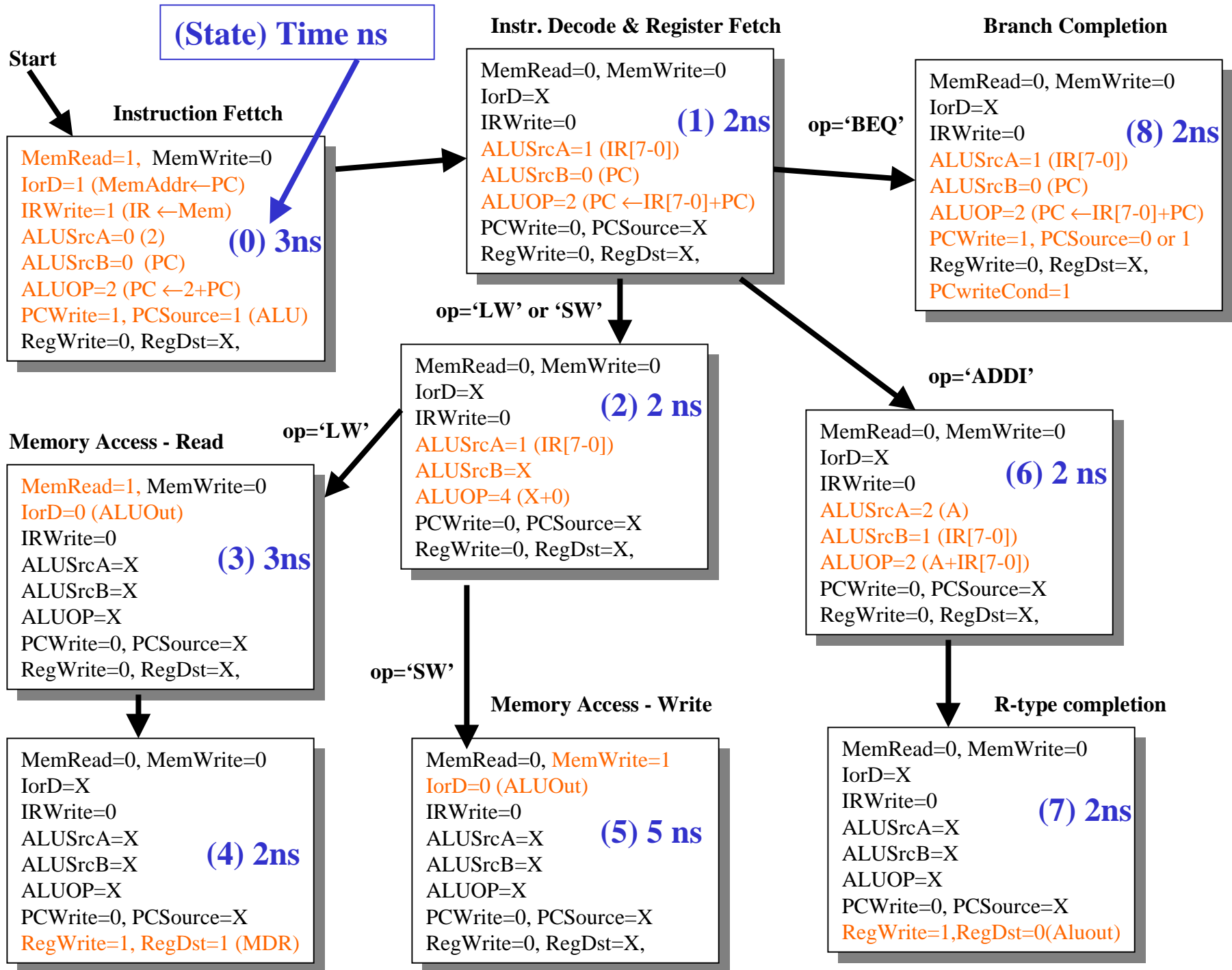
**(a, 20%)** Draw the finite state machine for RISCEE instructions (addi, load, store, beq).

**(b, 5%)**Place next to each state the amount of to process each state.

**see next page**

# RISCEE 2 Architecture







2 (c, 5%) Fill in critical path times for each instruction (copy delay times from part b).

Instruction	Instruction memory	Register Read	ALU operation	Data Memory	Register Write	Total Time	Clock Cycles
addi	3 ns	2 ns	2 ns		2 ns	9 ns	4
load	3 ns	2 ns	2 ns	3 ns	2 ns	12 ns	5
store	3 ns	2 ns	2 ns	5 ns		12 ns	4
beq	3 ns	2 ns	2 ns			7 ns	3

2 (d, 5%) Determine the fastest clock speed for the computer to work properly in frequency and show why.

**Clock period is the slowest resource in any one step: 5 ns**

**Clock frequency =  $1/\text{period} = 1/5\text{ns} = 200 \text{ Mhz}$**

**2 (d, 10%) Fill in the Clock, CPI, and MIPS in the above table and show all calculations.**

<b>Instruction</b>	<b>Clock Cycles</b>	<b>Instruction Mix</b>
<b>addi</b>	<b>4</b>	<b>40%</b>
<b>load</b>	<b>5</b>	<b>25%</b>
<b>store</b>	<b>4</b>	<b>10%</b>
<b>beq</b>	<b>3</b>	<b>25%</b>
<b>Clock speed</b>	<b>200 Mhz</b>	
<b>CPI</b>	<b>4</b>	<b>= <math>4*0.40+5*0.25+4*0.10+3*0.25</math></b>
<b>MIPS</b>	<b>50 MIPS</b>	<b>= <math>200 \text{ Mhz}/4</math></b>

**2 (f, 5%) Suppose you do not know the instruction mix. Explain which one functional unit (Memory write 5ns, Memory Read 3ns, Register 2ns, ALU 2ns) would you chose to improve by 1 ns and what will be the new clock speed? (show calculations)**

**The clock period is determined by the slowest resource at any one stage, which is in this case the memory write speed of 5ns.**

**Therefor improving the memory write from 5ns to 4ns will change the clock speed from  $1/5\text{ns}$  (=200Mhz) to  $1/4\text{ns}$  (=250Mhz).**



d) Convert the 5 bit signed binary 10010 into decimal

**For a signed number, the highest bit is a negative power**

**-16 8 4 2 1**

**Line up the bits:                    1 0 0 1 0**

**Then decimal is:                    -16+2 = -14**

e) Add 0x2 and 0xF and what is the overflow bit.

<b>Cin</b>	<b>1</b>	<b>1</b>	<b>0</b>		
	<b>0</b>	<b>0</b>	<b>1</b>	<b>0</b>	
	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>
<b>Sum</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>1</b>	
<b>Cout</b>	<b>1</b>	<b>1</b>	<b>1</b>		
<b>OV = 1^1 = 0</b>					

f) Multiply the 3 bit signed numbers 010 by 110 into a 6 bit signed number.

**First sign extend any negative numbers**

$$\begin{array}{r} 010 \\ 111110 \\ \hline 000 \\ 010 \\ 010 \\ 010 \\ 010 \\ 010 \\ \hline 010 \\ 111100 \text{ (only care about last 6 bits)} \end{array}$$

**Double check: 010 x 110 = 2 x -2**

**Double check product: 111100 is -32+16+8+4= -4**