EECS 322 Test 4 sample Wednesday April 12, 2000

Name: _____ Note: This exam is longer than the actual one

Problem 1. Show each step of the pipeline machine (page 540) for the following instruction sequence: Assume $1=9, $2=8; $3=5; $4=3; $5=2; Mem[12]=16

```
lw    $1, 4($2)
add   $3, $4, $5
nop
nop
```

Clock	<IF/ID> <PC, IR>	<ID/EX> <WB,M,EX,PC,A,B,S,Rt,Rd>	<EX/MEM> <WB,M,PC,Z, ALU, B, R>	<MEM/WB> <WB,MDR,ALU,R>
0	<0,?>	<?,?,?,?,?,?,?,?,?,?>	<?,?,?,?,?,?,?>	<?,?,?,?,?>
1				
2				
3				
4				
5				
6				
7				
8				

Problem 2. Assume a simple 6 stage pipeline with the following execution times

1	IF	Instruction fetch	3 ns
2	ID	Register Read	1 ns
3	EX	Multiply	4 ns
4	EX2	ALU	2 ns
5	MEM	Data Access	3 ns
6	WB	Register Write	1 ns

This computer has the following instructions:

Instruction		Operation
add	$rd, $rs, $rt	$rd = $rs + $rt
lw	$rt, addr16($rs)	$rt = Mem[addr16+$rs]
sw	$rt, addr16($rs)	Mem[addr16+$rs]=$rt
beq	$rs, $rt, disp16	pc = pc+2+($rs-$rt=0?disp16:0)
madd	$rd, $rs, $rt	$rd = $rs*$rt + $rd

(a) Fill in the following table

Instruction	IM	ID	EX	EX2	MEM	WB	Total Time	Multi-Cycles	Instruction Mix
add									20%
lw									20%
sw									20%
beq									20%
madd									20%

(b) Fill the following table

Instruction	Clock frequency	CPI	MIPS
Single-cycle CPU			
multi-cycle CPU			

The parts refer to pipelined machine only

(c) What is the instruction latency?

(d) What is the pipeline clock?

(e) What is the pipelined speed up?

(f) Without forwarding, fill in the hazard type (page 441-8) and condition (page 479), for the following instruction sequence:

Instruction	Hazard type and condition
add $1, $2, $3	
sub $4, $2, $1	
lw $5, data($6)	
beq $1, $5, loop2	

(g) Without forwarding, draw the pipeline sequence (like figure 6.4) for part f
(h) .Show all timing, including stalls.

(i) Suppose the hazard detection unit does not work on the processor due to a bug in the design. Using the nop instruction, rewrite the code of part f which will give correct results (like page 478).

(j) Using forwarding, draw graphical pipeline sequence (like figure 6.8) of part f. Show all shading.
(k) Show all timing including stalls.

(l) Using forwarding, reorder the code to minimize the stalling of part f.

(m) Given any 2 instruction combinations, what is the worst instruction sequence. (i.e. assume no forwarding or prediction). Draw the pipeline chart (like Figure 6.4). Determine the MIPS.

(n) Given any 2 instruction combinations, what is the worst instruction sequence using forwarding. Draw the pipeline chart (like Figure 6.4). Determine the MIPS.

(o) Using all the best possible instruction flow (i.e. no hazards, assume no forwarding or prediction) of the 5 instructions. Determine the MIPS.

(p) Show the worst possible instruction pipeline sequence of using only the 5 instructions. (i.e. assume no forwarding or prediction). Draw the pipeline chart (Figure 6.4). Determine the MIPS.