EECS 317: *Computer Design*

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Objective To introduce and expose the student to methodologies for systematic design of digital systems with emphais on programmable logic implementations and prototyping. The course requires a number of hands-on lab experiments and an overall lab project. The Lab involves a number of class lectures, once per week, to familiarize the students with the modern design techniques based on VHDL, CAD tools and FPGAs. However, the essential part of this course is an advanced laboratory which is currently in operation in room 411 Olin. The Lab facility is organized into a number of Lab units, currently 6 units. Each Lab unit is equipped with a Xilinx and Altera FPGA-based board, a Sun Blade 100 workstation running the Synopsys CAD tools, the Xilinx FPGA configuration tools, and the Altera FPGA CAD software. The Lab has been recently equiped with a number of advanced Nios FPGA boards from Altera together with microporcessor software based on the ARM core. The Nios FPGA chip are equivalent to 250K gates and can easily accommodate an ARM-based design. Moreover, GNU compiler tools can be used to generate embedded software for the configurable hardware designs. Other miscellaneous equipment include prototype board(s), a number of PCs, PC Lab interface boards, Logic Analyzers, and other components.

Outline

- **Course Topics**

  1. Review of Logic Design.
  2. Digital Design using VHDL.
  3. VHDL Simulation and Synthesis using the Synopsys CAD software.
  4. Introduction to Programmable Logic – PLAs, PALs, PLDs, FPGAs.
  5. Design Techniques using programmable logic – partitioning, block assignment routing.
  6. Digital System Design – Datapath and Controllers.
  7. Digital System design using advanced FPGAs. Emulation and Rapid Prototyping.

- **Laboratory**

  1. Design of a combinational logic circuit on FPGAs. Design Steps. a) VHDL Simulation and Syntesis of the design. b) Download the design configuration on the FPGA board. c) Hardware debugging. Examples are, ALU, Decoder, barrel shifter. Lab report required.
  2. Design of state machine controllers using FPGAs. Examples: Traffic Control System, Security Alarm System, Vending Machine Controller, etc. Lab report required.
  3. Lab Project. Design of a real-world digital system using the system design flow discussed in class. Start from VHDL specification, go through RTL synthesis, FPGA mapping, and FPGA emulation. Actually built a system hardware bread board and test it. A technical report and demo is required.

- **Prerequisite**: EECS 281 (hard), EECS 315 (soft – waved by instructor).