

EECS 317: *Computer Design*

Instructor: *Chris Papachristou*

Room 502 Olin, 216-368-5277, cap@alpha.ces.cwru.edu

Objective To introduce and expose the student to methodologies for systematic design of digital systems with emphasis on programmable logic implementations. The course requires a number of hands-on lab experiments and an overall lab project. An advanced laboratory is currently being built to enhance this course. The lab facility will include a number of Lab units, each equipped with a Xilinx or Altera FPGA-based board, a Sparcstation running Synopsys CAD tools and Xilinx FPGA configuration tools, hardware prototype board(s), a PC interfaced to the boards, an HP Logic Analyzer, and other components.

• **Outline**

• **Course Topics**

1. Review of Logic Design.
2. Logic and State Machine Synthesis.
3. Digital Design using VHDL.
4. Introduction to Programmable Logic – PLAs, PALs, PLDs, FPGAs.
5. Design Techniques using programmable logic – partitioning, block assignment routing.
6. Digital System Design – Datapath and Controllers.
7. Digital System design using advanced FPGAs. Emulation and Rapid Prototyping.

• **Laboratory**

1. Design of a combinational logic circuit on FPGAs. Examples are, ALU, Decoder, barrel shifter. Lab report required.
2. Design a state machine controller using FPGAs. Examples: Traffic Control System, Security Alarm System, Vending Machine Controller, etc. Lab report required.
3. **Lab Project**. Design of a real-world digital system using the system design flow discussed in class. Start from VHDL specification, go through RTL synthesis, FPGA mapping, and FPGA emulation. Actually built a system hardware bread board and test it. A technical report and demo is required.