



EECS 318 CAD
Computer Aided Design

LECTURE 1: Introduction

CAD Design approaches

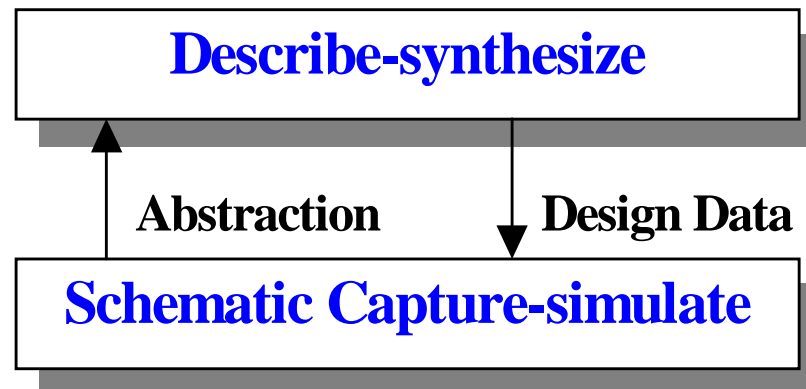


- Goal of each CAD design flow methodology is to **increase productivity** of the design engineer
- Increasing the **abstraction level** of the design methodology and tools is one approach:

Gates/eng./month

1.5K - 6K

300 - 600



Design Sizes

> 1M gates

100K - 500K gates

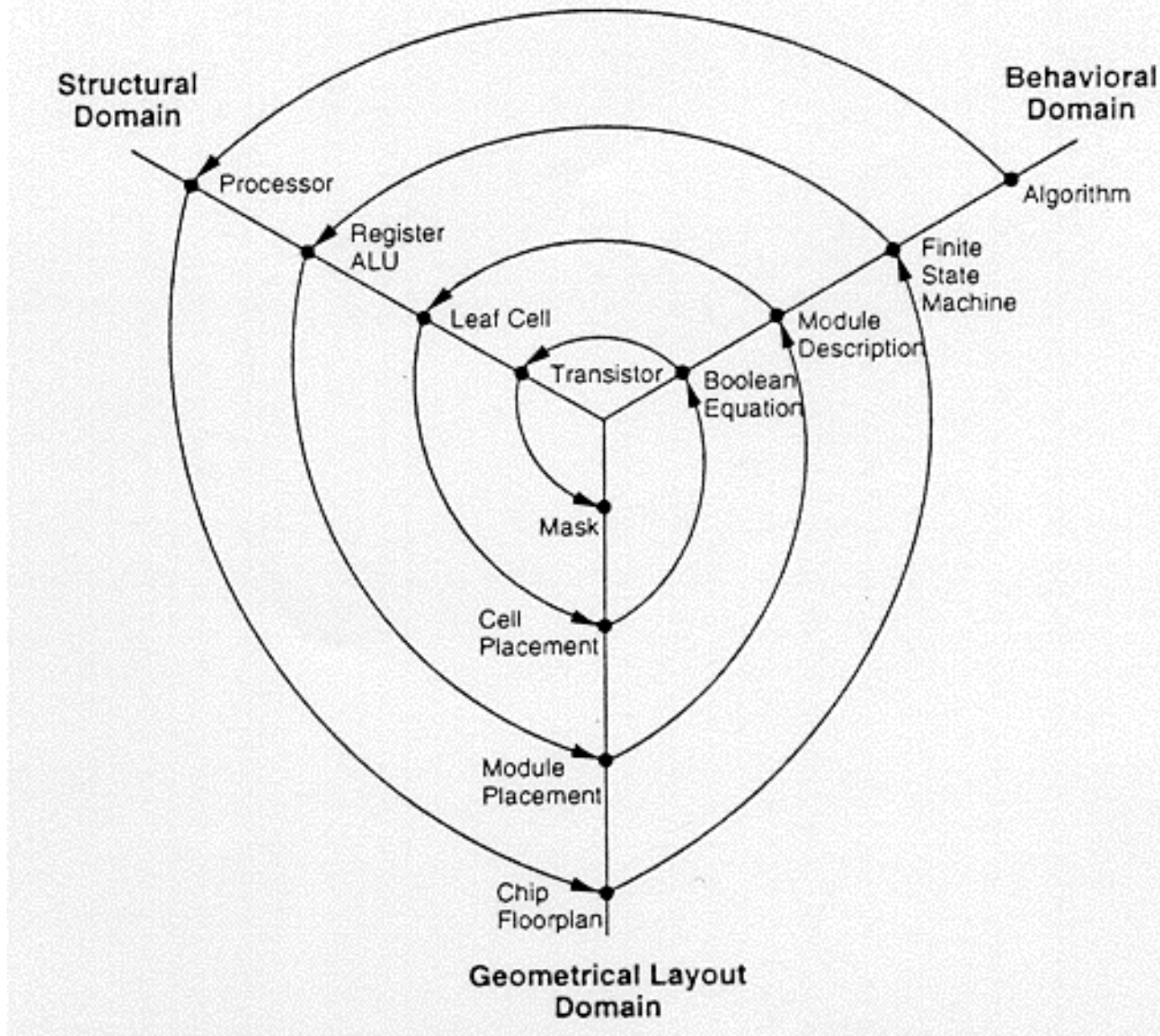
SoC: System on a Chip



- The 2001 prediction: SoC's will be > 12M gates
- How do you create million gate ASICs with same amount of resources?
 - ...while
 - Decrease development time
 - Increase functionality and performance
 - Keep small design teams
 - Design Methodology (Design flow)
 - Tools that support the Methodology
 - IP reuse (Intellectual Property)

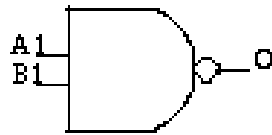


ASIC and SoC Design flow

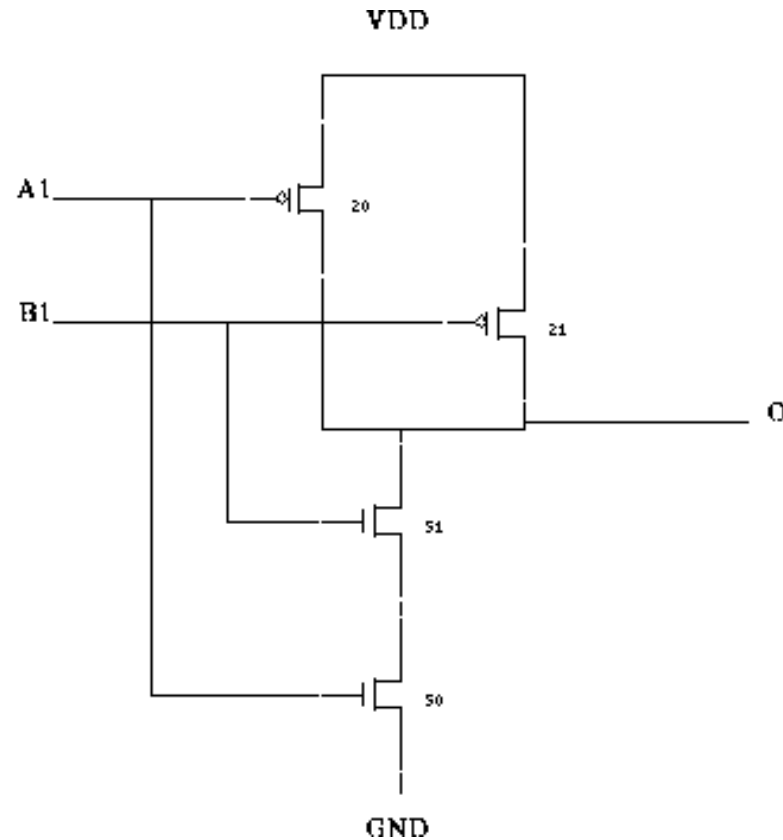


Nand gate: behavioral, transistor, layout

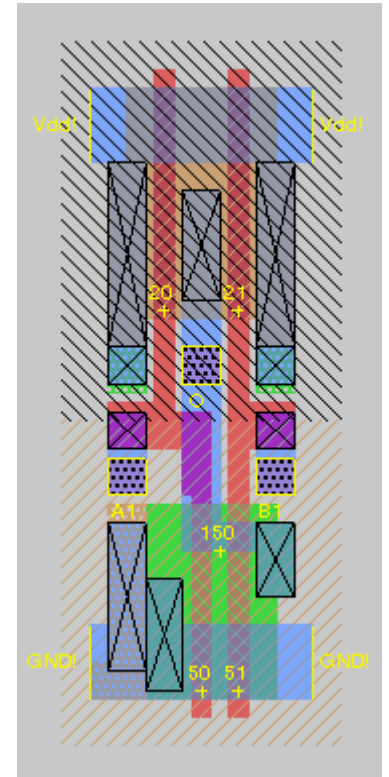
$O \leftarrow \text{NOT} (A1 \text{ AND } B1);$



Boolean Equation



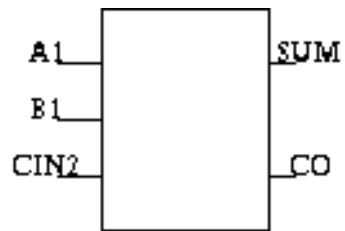
Transistor



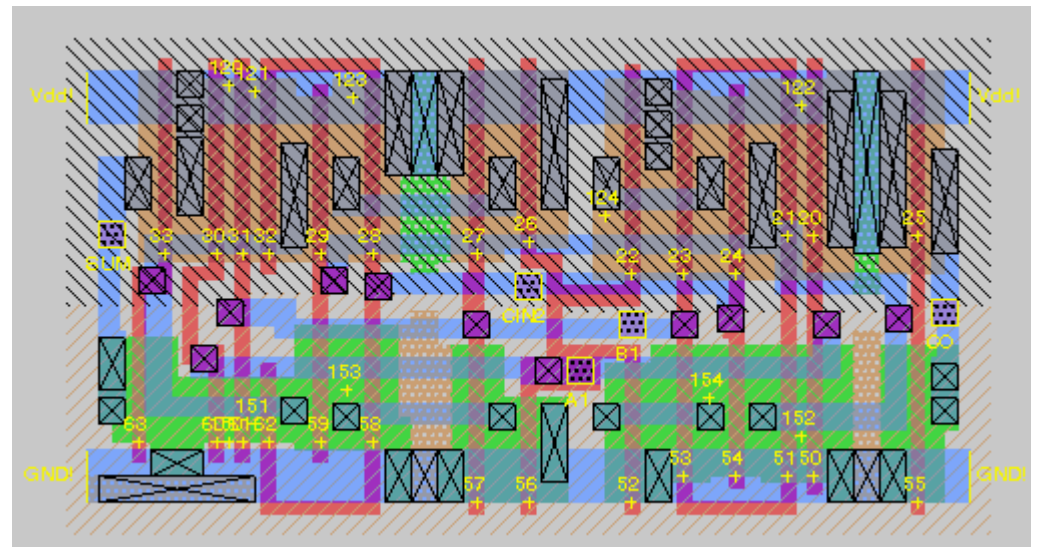
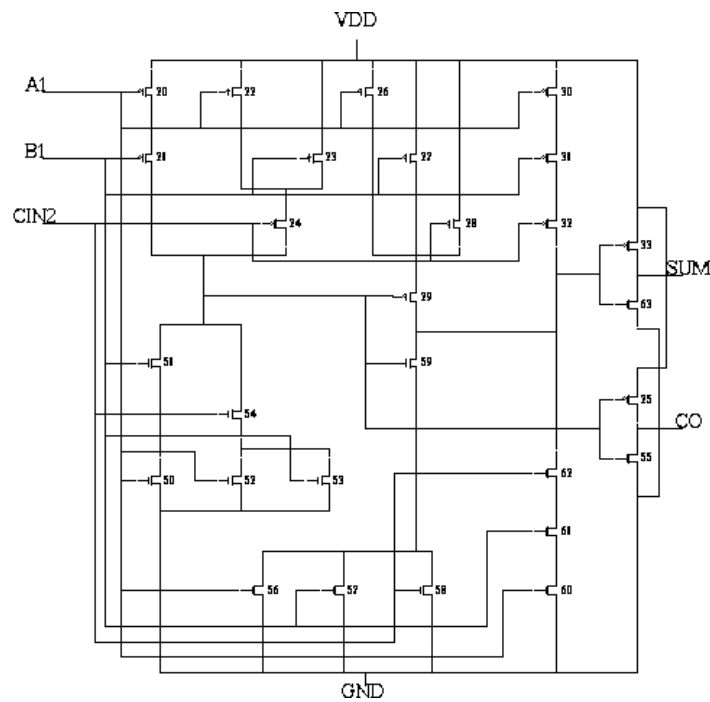
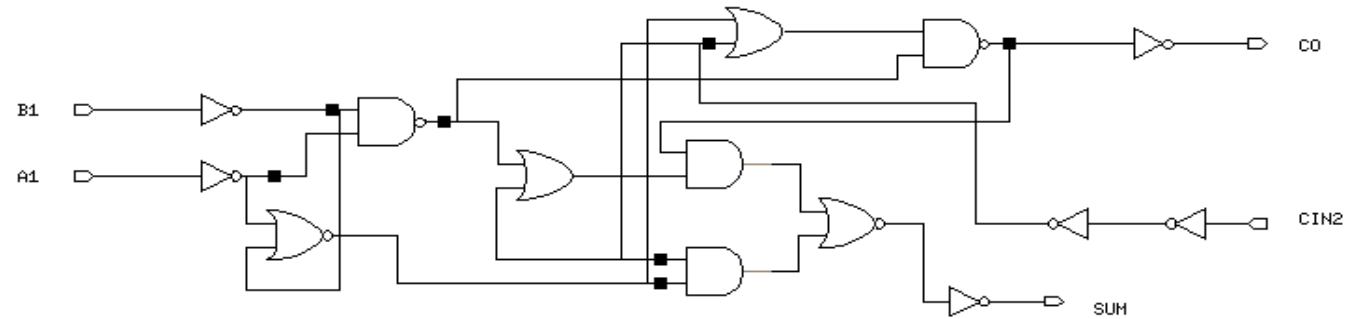
Mask

Adder: behavior, netlist, transistor, layout

Behavioral model



Structural model



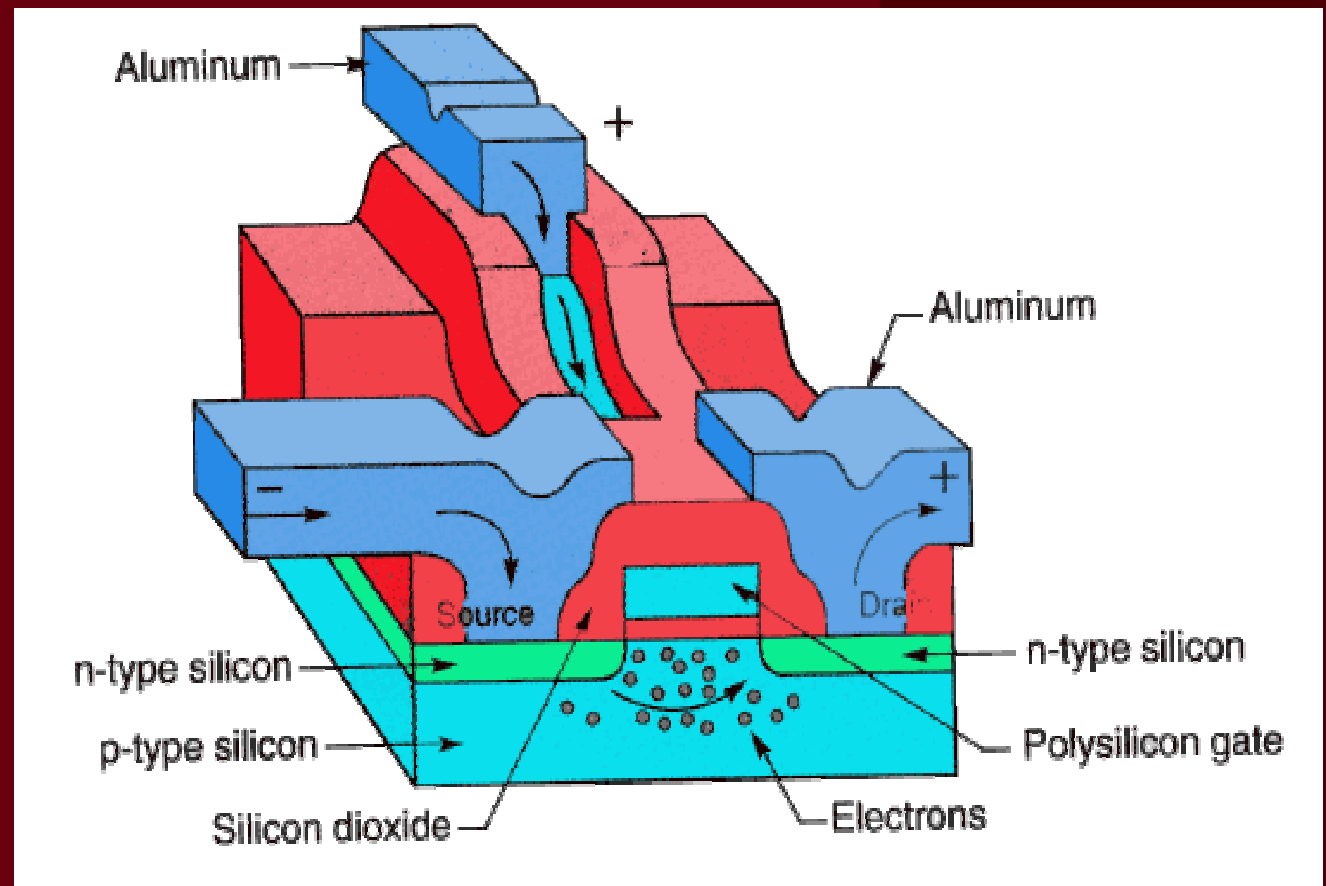
Review



- **To appreciate why we need high level design techniques**
- **We need to look over the past 30 years of chip development and their growing complexity**

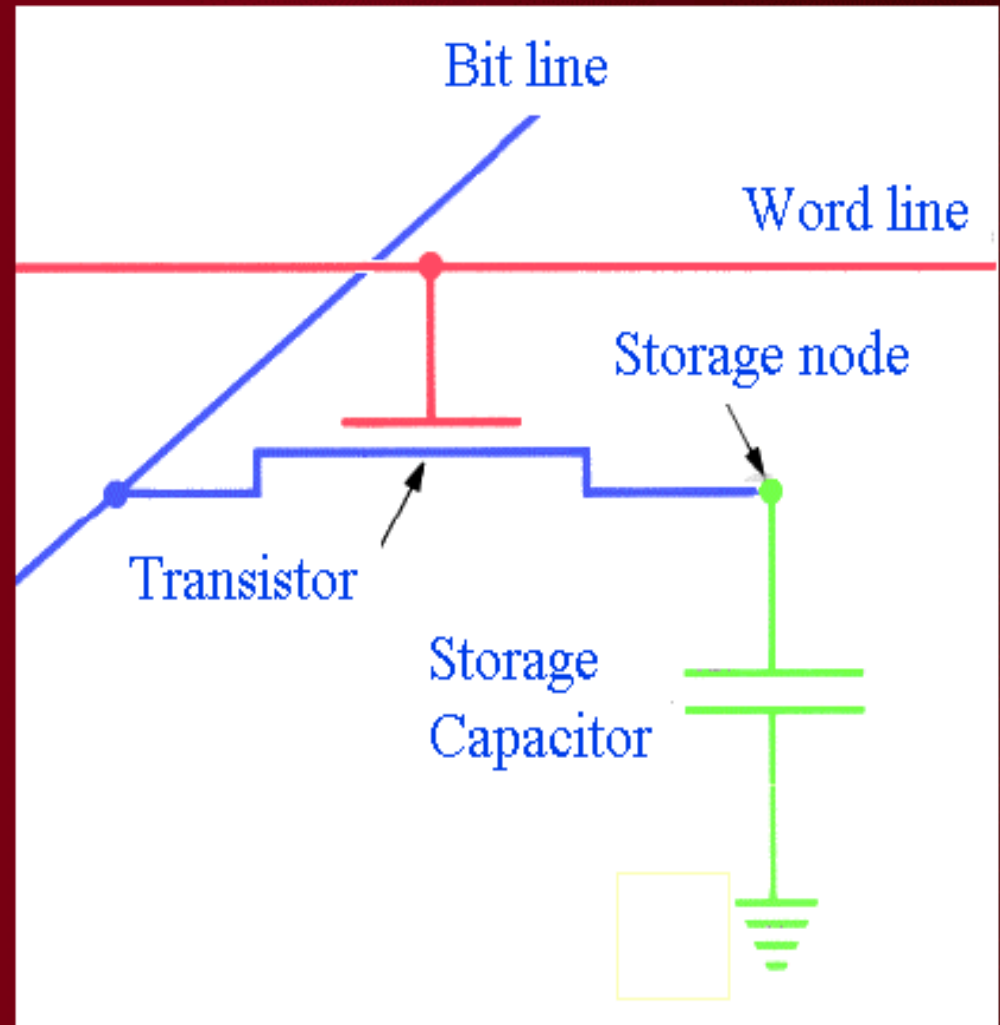
Real transistor

- 3-D structure
- Real materials



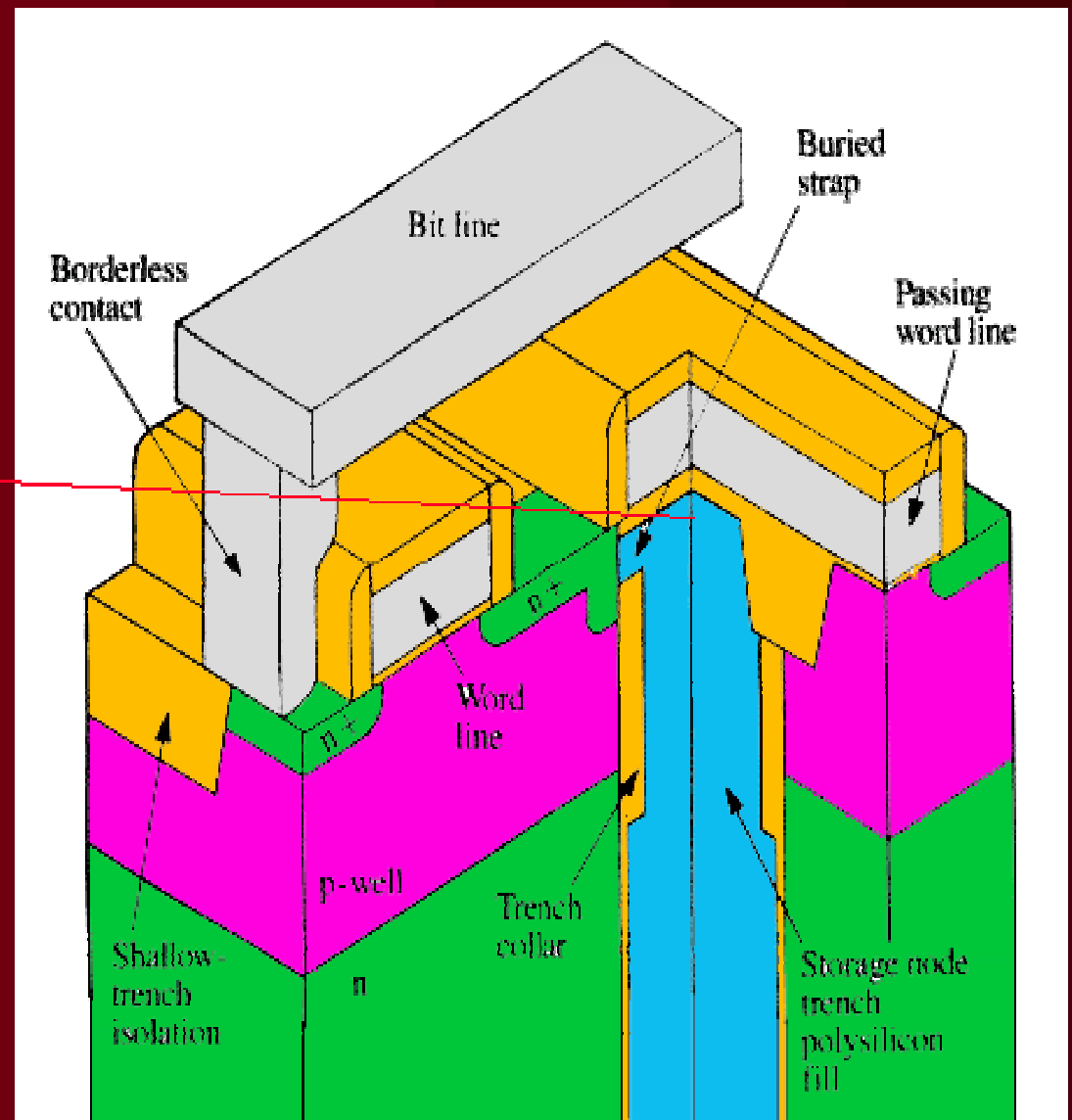
Basic DRAM design

- DRAM replaces all but one transistors of flip-flop with a capacitor
- => smaller!
- Capacitor stores information
- Charge leakage requires periodic refreshment (sense & rewrite)



256Mb DRAM

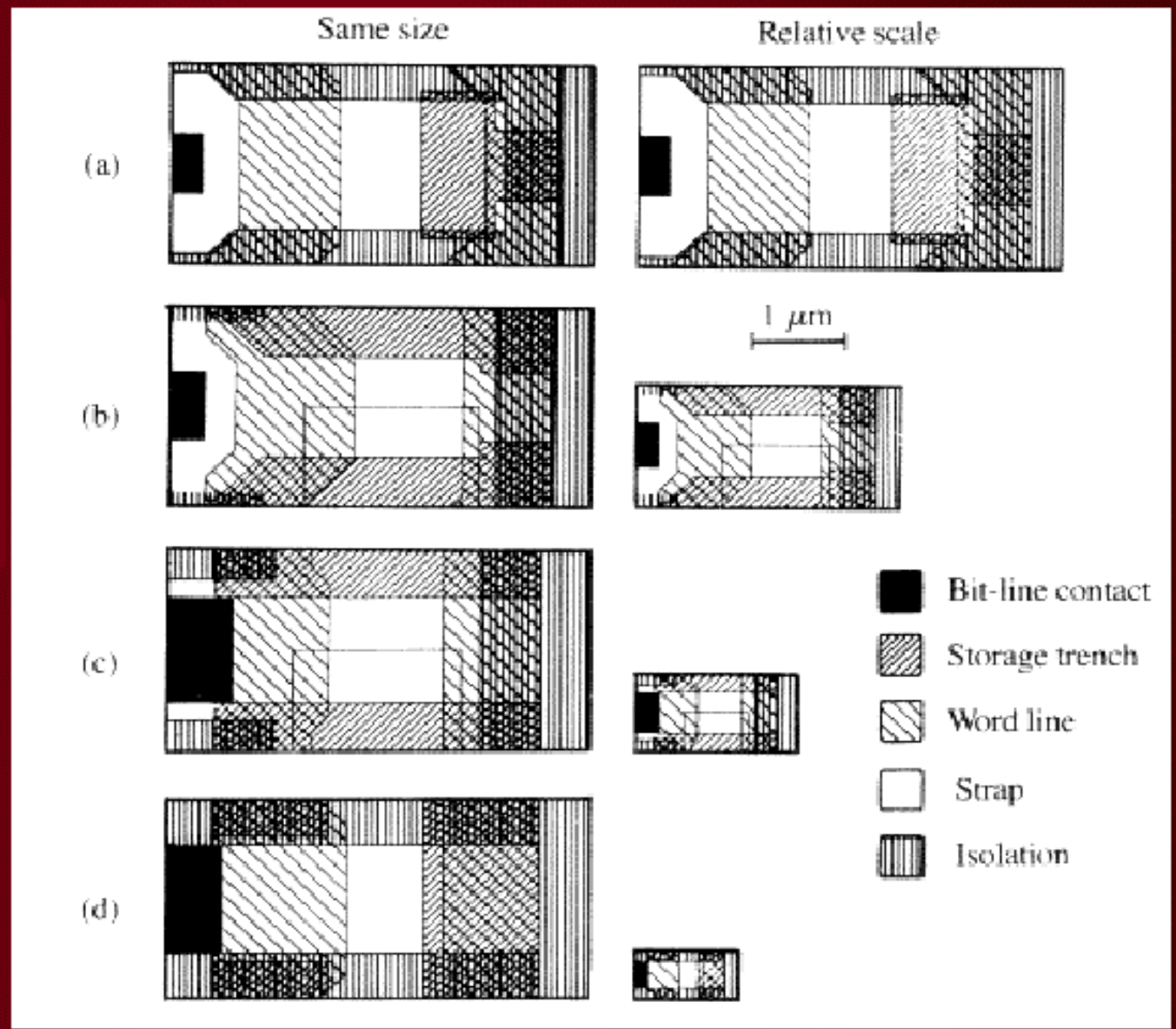
- Increased vertical integration
- Word line passes over capacitor and contact
- Cell area $\sim 0.5\mu\text{m}^2$
- Capacitor area smaller - dielectric must be thinner
- => higher quality dielectric required



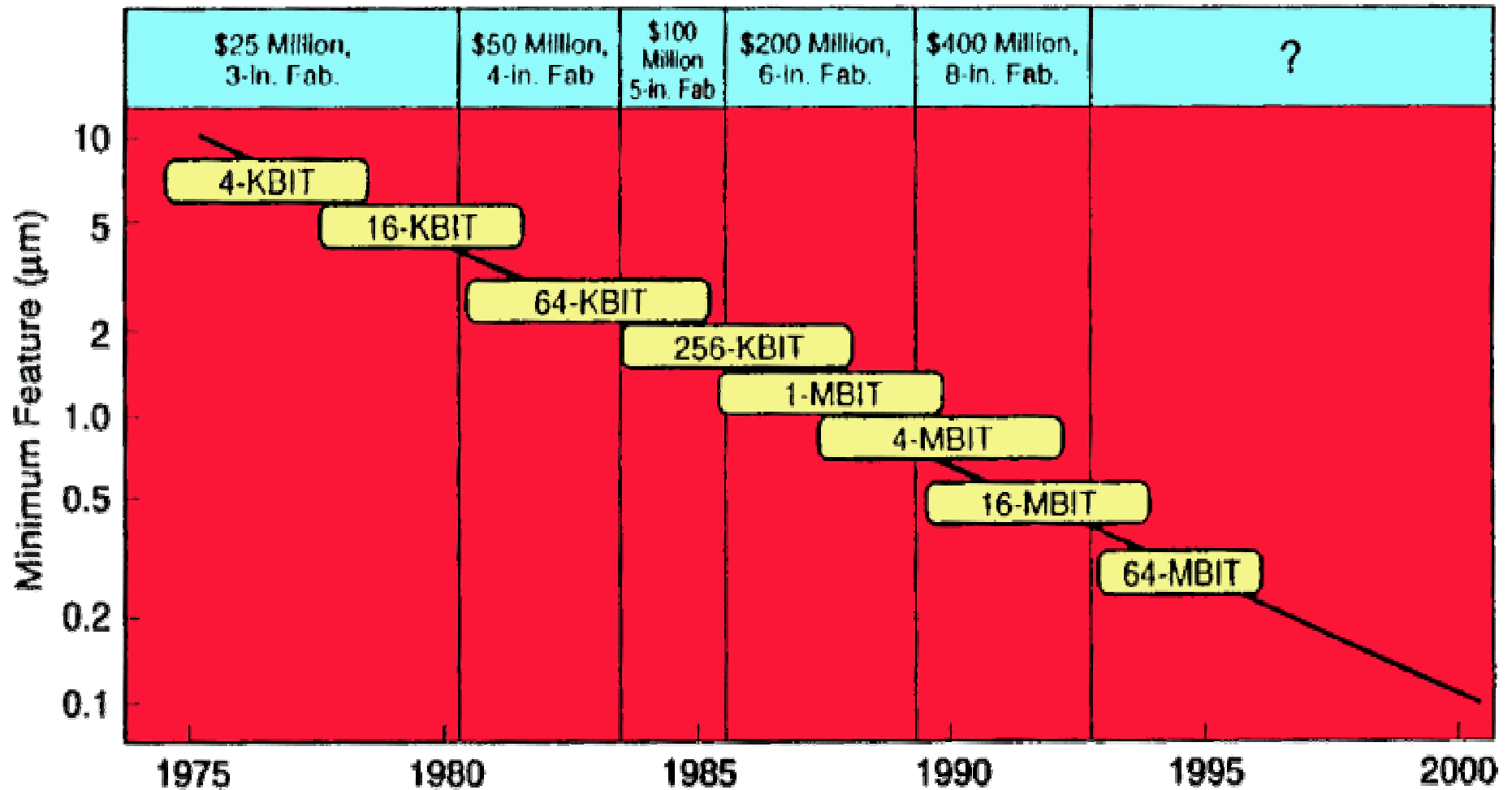
Memory Technology: DRAM Evolution



DRAM evolution (II)

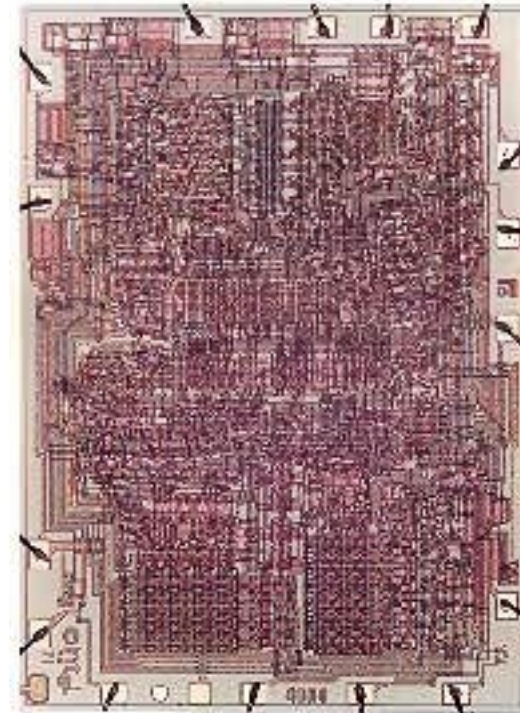
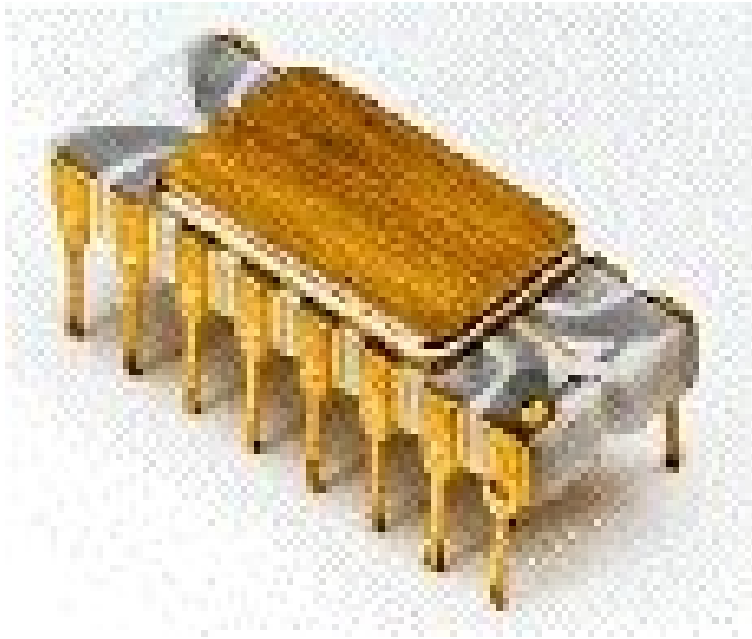


DRAM development



SoC: Intel Microprocessor History: 4004

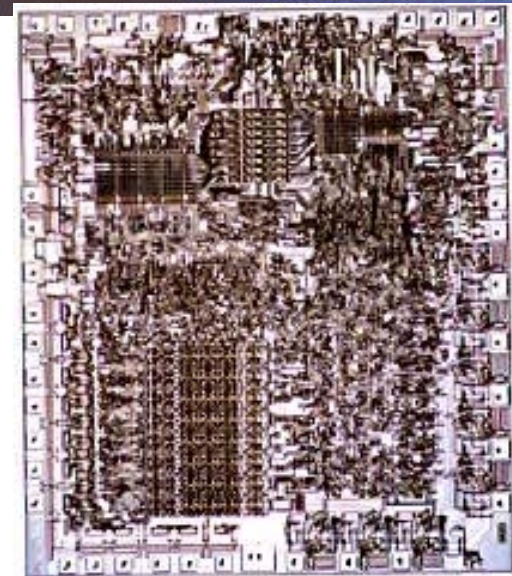
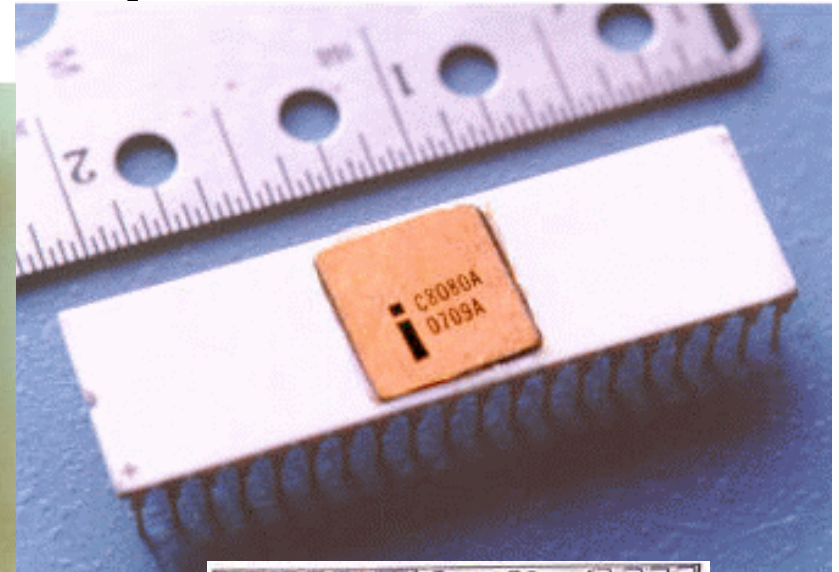
- 1971 Intel 4004, 4-bit, 0.74 Mhz, 16 pins, **2250 Transistors**



- Intel publicly introduced the world's first single chip microprocessor: U. S. Patent #3,821,715.
- Intel took the integrated circuit one step further, by placing CPU, memory, I/O on a single chip

SoC: Intel Microprocessor History: 8080

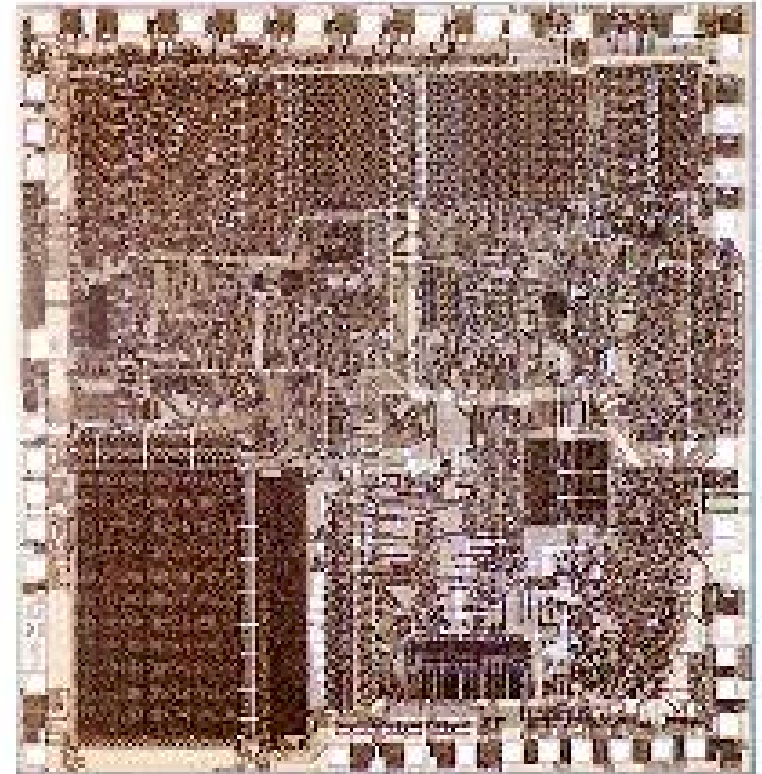
- 1974 Intel 8080, 8-bit, 2 Mhz, 40 pins, **4500 Transistors**



**Bill Gates & Paul Allen
write their first Microsoft
software product: Basic**

SoC: Intel Microprocessor History: 8088

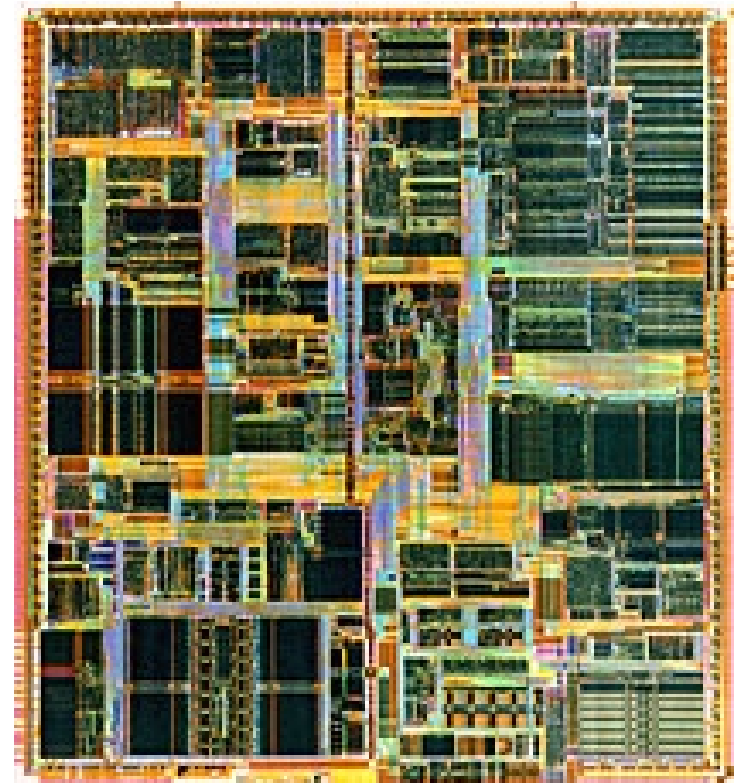
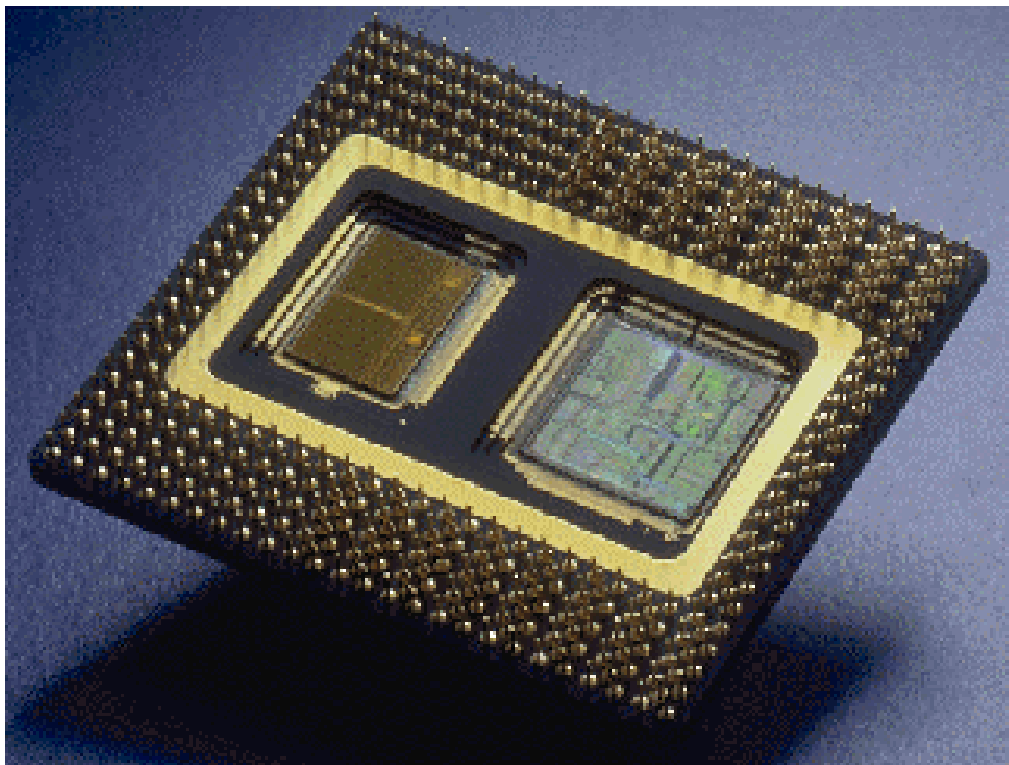
- 1979 Intel 8088, 16-bit internal, 8-bit external, 4.77 Mhz, 40 pins, **29000 Transistors**



- **0.128M - 0.640M RAM**
- **0.360Kb, 5.25" Floppy**
- **10M Hard Disk**

SoC: Intel Processor History: Pentium Pro

- 1995 Intel Pentium Pro, 32-bit ,200 Mhz internal clock, 66 Mhz external, Superpipelining, 16Kb L1 cache, 256Kb L2 cache, 387 pins, **5.5 Million Transistors**

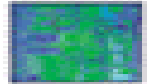


Intel's microprocessor evolution

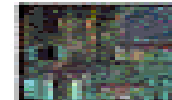
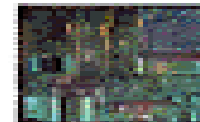
silicon process technology

1.5 μ 1.0 μ 0.8 μ 0.6 μ 0.35 μ 0.25 μ

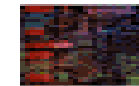
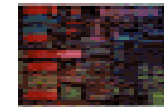
Intel® Pentium® III processors



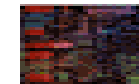
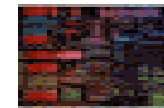
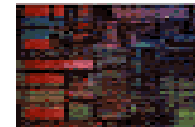
Pentium® II processors



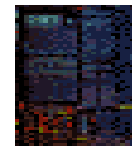
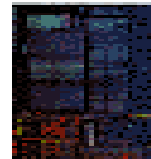
Pentium® Pro processor



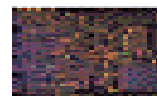
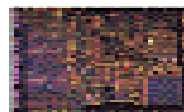
Pentium® processor



Intel486™ DX processor



Intel386™ DX processor



SoC: System on a chip (beyond Processor)

- The 2001 prediction: SoC's will be > 12M gates

