

EECS 318 CAD Computer Aided Design

LECTURE Simulator 2: Textio, Wait, Clocks, and Test Benches

Sopwith
Camel
SOP.1086

Instructor: Francis G. Wolff
wolff@eecs.cwru.edu

Case Western Reserve University

This presentation uses powerpoint animation: please viewshow

adder_full_tb_io.vhd: full adder test bench



```
use STD.TextIO.ALL;  
LIBRARY IEEE;  
use IEEE.std_logic.all;  
use IEEE.std_logic_textio.all;
```

Note: in order to use i/o, additional libraries must be included

```
ENTITY adder_full_tb_io IS  
END;
```

This test bench contains no outputs

adder_full_tb_io.vhd: architecture begin



```
ARCHITECTURE adder_full_tb_io_arch
    OF adder_full_tb_io IS
    COMPONENT adder_full
        PORT (x,y,Cin: IN std_logic; Sum,Cout: OUT std_logic);
    END COMPONENT;

    SIGNAL x, y, Cin, Sum, Cout: std_logic;
BEGIN

    UUT_ADDER: adder_full PORT MAP(x, y, Cin, Sum, Cout);
```

adder_full_tb_io.vhd: test case #1



PROCESS

VARIABLE **S**: LINE; --used for write line buffer

BEGIN

-- Test Case #1

x <= '0'; **y** <= '1'; **Cin** <= '0';

WAIT FOR 5 ns;

WRITE(**S**,STRING(" X="));

WRITE(**S**, **x**);

WRITE(**S**,STRING(" Y="));

WRITE(**S**, **y**);

WRITE(**S**,STRING(" Cin="));

WRITE(**S**, **Cin**);

WRITE(**S**,STRING(" Sum="));

WRITE(**S**, **Sum**);

WRITE(**S**,STRING(" Cout="));

WRITE(**S**, **Cout**);

WRITELINE(OUTPUT, **S**);

adder_full_tb_io.vhd: test case #2



-- Test Case #2

```
x<= '1'; y<= '1'; Cin<= '0';
```

```
WAIT FOR 5 ns;
```

```
WRITE(S,STRING(" X="));
```

```
WRITE(S,STRING(" Y="));
```

```
WRITE(S,STRING(" Cin="));
```

```
WRITE(S,STRING(" Sum="));
```

```
WRITE(S,STRING(" Cout="));
```

```
WRITELINE(OUTPUT, S);
```

```
WRITE(S, x);
```

```
WRITE(S, y);
```

```
WRITE(S, Cin);
```

```
WRITE(S, Sum);
```

```
WRITE(S, Cout);
```

adder_full_tb_io.vhd: configuration



```
ASSERT FALSE
    REPORT "Simulation Done"
    SEVERITY ERROR;
END PROCESS;
END ARCHITECTURE;

CONFIGURATION adder_full_tb_io_cfg OF
    adder_full_tb_io IS
    FOR adder_full_tb_io_arch
    END FOR;
END CONFIGURATION;
```

VHDL Simulator: running the test bench



```
Unix> vhdlan -NOEVENT adder_full.vhd
```

```
Unix> vhdlan -NOEVENT adder_full_tb_io.vhd
```

```
Unix> vhdlsim WORK.adder_full_tb_io_cfg
```

```
# ls
```

```
ADDER_FULL_TB_IO STANDARD ATTRIBUTES  
STD_LOGIC_1164 _KERNEL
```

```
# run
```

```
X=0 Y=1 Cin=0 Sum=1 Cout=0
```

```
X=1 Y=1 Cin=0 Sum=0 Cout=1
```

```
10 NS
```


```
Assertion ERROR at 10 NS in design unit
```

```
ADDER_FULL_TB_IO(ADDER_FULL_TB_IO_ARCH) from  
process /ADDER_FULL_TB_IO/_P0:
```

```
"Simulation Done"
```

```
# quit
```

VHDL clock behavioral component



```
ENTITY clock_driver IS
    GENERIC (Speed: TIME := 5 ns);
    PORT (Clk: OUT std_logic);
END;
```

```
ARCHITECTURE clock_driver_arch OF clock_driver IS
    SIGNAL Clock: std_logic := '0';
BEGIN
    Clk <= Clk XOR '1' after Speed;
    Clock <= Clk;
END ARCHITECTURE;

CONFIGURATION clock_driver_cfg OF clock_driver IS
    FOR clock_driver_arch END FOR;
END CONFIGURATION;
```


Team Assignment #5 Test benches (1/2)



- Display all input and output bits
- Three tests with correct results for each test bench
- Cut and Paste the output to a file and print it

System Level: Team member #1 is responsible for

- T101_ALU_BIT_TB.vhd and T101_ALU_TB.vhd

Processor: Team member #2 is responsible for

- T101_FSM_TB.vhd: test bench for add instruction

Memory: Team member #3 is responsible for

- T101_RAM_TB.vhd write and read some words
- T101_ROM_TB.vhd with machine instructions

Team Assignment #6 System Test Bench



The report should contain the following

- Cover sheet
- Each entity section should have the
 - vhdl, simulation, and synthesis
- The vhdl T101_PU_TB.vhd test benches
 - Simulate the 32 bit add program: $output = input + 1$
 - Read first byte value from the input port and zero upper 24 bits via lbi's
 - Load the second value from immediate loads
 - Store the results in the output port
 - Display the output port in the test bench
- Combined report of Assignments #3, #4, #5
- Everything is due Thursday October 26!