Soft Delay Error Analysis in Logic Circuits

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***Abstract*— In this paper, we present an analysis methodology to compute circuit node sensitivity due to charged particle induced delay (timing) errors, Soft Delay Errors (SDE). We define node sensitivity metric and describe a step by step procedure to compute node sensitivity. We use mixed-mode simulations to extract accurate current pulses for the characterization of SDE. A technique for logic cell library characterization for SDE is described. Our approach is orders of magnitude faster than using Spice based analysis and its accuracy is close to Spice. Using our approach, we provide distribution of nodes sensitivity for various ISCAS85 circuits and two adders. Such analysis is important to employ node hardening techniques on selected nodes to increase the reliability of CMOS circuits. We use two test circuits to apply a node hardening technique on the highly sensitivy nodes which were determined by our approach. Results are provided for the reduction of the circuit sensitivity.**

I. Introduction

As the process technology scaling down, the reliability of nano-meter circuits is decreasing. Soft errors due to radiation-induced upsets are becoming a major reliability concern in nano-meter circuits. These upsets originate from two primary sources: cosmic ray particles occurring in the space environment and alpha particles emitted from radioactive decay of uranium and thorium impurities located within the chip itself such as the silicon die, interconnects, and ceramic packaging. Soft errors have been a known problem in semiconductor memories for quite some time. However, due to faster clock rates and shrinking process technologies soft errors are now affecting CMOS logic [1], [2], [3], [4], [5]. A recent study shows that the projected soft error rate in logic will dominate in microprocessors [3].

Some of the known effects of radiation-induced upsets in logic are: Single Event Transients (SET) [1], [2], Radiation Induced Clock Jitters (RIJ) and Race (RIR) [6], and Soft Delay Errors (SDE) [7]. These errors occur under certain conditions of the circuit. SET occurs when the particle generated glitch can propagate to the circuit output(s) and is captured by the flip-flop(s). RIJ occurs when the particle strike upsets the latching edge of the clock. RIR occurs when particle strike generates a new clock edge. SDE occurs when the particle strike during the signal transition induces delay such that the affected signal arrives at the output much later than expected and the wrong value is captured by the flip-flop.

Motivation - The circuit failures due to RIJ, RIR, and SDE have been reported in the literature recently. So far, SET are considered the main cause of transient failure of combinatorial circuits. However, for mission critical application such as avionics [8], medical systems - heart defibrillators [9], etc., where the reliability is the most important objective over the cost and the performance, RIJ, RIR, and SDE must be considered. The focus of this paper is on SDE analysis.

Increasing the clock rate of circuits results in increasing the number of the transition events at the circuit nodes which increases the probability of the occurrence of SDE. Moreover, the reduction of the charge stored at the circuit nodes increases the failure rate of the circuit due to soft errors because even low energy particles can cause upsets. The frequency of the occurrence of low energy particles is much higher than the one for high energy particles [10].

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The failure rate of a circuit due to soft errors, Soft Error Rate (SER), depends on the sensitivity of the circuit nodes to the radiation-induced upsets. A circuit node is the drain of the transistor sensitive to the particle strike. The node sensitivity is non-uniform in nature as it depends on the transistor strength, capacitive load at node, V_{dd} value, etc. Moreover, it depends on the probability of the input state of the circuit which sensitized distinct data paths. The SER of a circuit can be reduced by using circuit hardening techniques but this can result in unacceptable design overhead. Hence, by analysis and quantifying the node sensitivity, we can employ appropriate techniques to reduce the sensitivity of highly sensitive nodes which will lead to the reduction of the SER of the overall circuit.

Researchers have developed techniques for the node sensitivity analysis for soft errors in CMOS circuits based on propagation of the charged particle induced glitches (i.e. SET) [1], [2], [11], [12], [13]. However, analysis techniques for the glitch propagation cannot be directly applied for SDE analysis because the masking effects on SET are different than SDE. In this paper, our key contribution is a novel approach for the node sensitivity analysis for SDE.

Related work - Soft errors and transient fault propagation in combinational circuits have been studied in [1], [2], [3], [12], [13], [14]. Many factors which effect the soft delay in CMOS logic circuits such as technology scaling, V_{dd} scaling, transistor strength and gate fanout were discussed in [7]. To the best of our knowledge, this is for the first time that a node sensitivity analysis approach for soft delay error is introduced in this paper.

This paper is divided into following sections. Section II discusses the occurrence of soft delay in CMOS circuits. Soft delay errors in logic in contrast to SET are discussed in III. Section IV presents our approach for the node sensitivity analysis for SDEs. Section V provides results for various ISCAS85 benchmark circuits using our approach. We conclude in section VI.

II. Background

A Single Event Upset (SEU) in semiconductor devices occurs due to a charged particle strike at a sensitive node. In case of CMOS circuits, a sensitive node is the drain of the OFF-transistor. The particle strike creates electron-hole pairs on its track. The drift and the diffusion of electron-hole pairs generates a current pulse. The duration and the amplitude of the current pulse depend on the striking particle energy, the transistor strength, the load capacitance, and the V_{dd} value. This pulse can have positive or negative magnitude depending on whether the particle hits at the drain of the OFF NMOS or PMOS transistor. For transient simulations of the circuit for SEUs, the charge collection process is accounted for in our simulations by a current source connected between the circuit node and its substrate [3], [14].

During the rising (falling) phase of a transition at the output of a gate in CMOS circuits, the NMOS (PMOS) transistor goes to OFF state and the PMOS (NMOS) goes to ON state. As soon as the NMOS (PMOS) transistor turns off and the p-n junction between the drain and the substrate of the NMOS (PMOS) transistor is reverse biased, it becomes sensitive to a particle strike. If the particle hits on

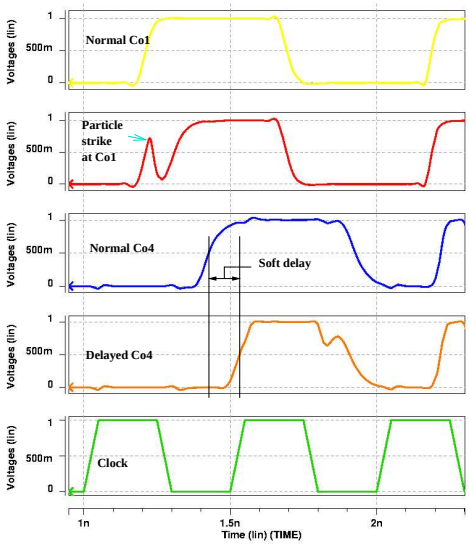

Fig. 1. Soft delay error in a 4-bit ripple carry adder.

this sensitive node during the signal transition, the current generated due to the hit can pull down the signal in the direction of opposite logic level causing longer transition time. This longer transition of the signal at the node can have a delay effect, soft delay, at the output of the succeeding gate(s). An erroneous information will be latched by the output flip-flop if the delayed signal propagates to the observable output(s) of the circuit and violates the setup time of the flip-flop which is called Soft Delay Error (SDE).

Figure 1 shows the Hspice simulation result for a particle strike induced delay in a 4-bit ripple carry adder. This circuit was placed between input and output clocked flip-flops. From the top in Figure 1, the first signal, $Co1$, is the carry output of the first stage of the adder which is in rising phase of the transition. The second signal occurs when the particle strikes during the transition at $Co1$ which increases the transition time. This longer transition results in delay at the carry output of the last stage of the adder, $Co4$ which constitutes the soft delay. In this case, the delayed $Co4$ produces SDE as it arrives during the setup time of the output flip-flop (not shown in Figure 1) and results in incorrect data latchup.

As the process technology shrinks and supply voltage decreases, the charge stored at nodes of logic circuits decreases because $Q_{node} = C_{node} \times V_{dd}$, which is one of the reasons of increasing sensitivity of nodes for soft errors or SDEs. As the operating frequency of circuits increases the signal transition events at nodes are also increasing which increases the probability of SDEs. Thus, in Very Deep Sub-Micron (VDSM) technologies SDEs in logic circuits can become a reliability problem.

III. Soft Delay Errors Versus Glitch Errors

A. Soft Delays in Logic

When a particle strikes at the semiconductor device, it losses energy as it travels through the devices and comes to rest after losing all of its energy. The energy loss per unit length is called Linear Energy Transfer (LET) and is expressed in $MeVcm^2/mg$. We used device simulations for the 100nm process technology to obtain current pulses generated by the particles strike for various values of the LET. Alternatively, these current pulses can be obtained from the analytical models of the current pulse as used in [3], [12]. The main advantage of using device simulations is that the accurate shape of the current pulses can be obtained for the given process technology

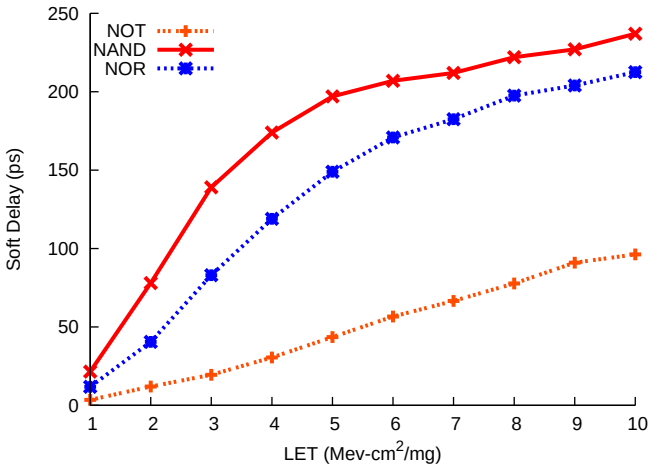

Fig. 2. Soft delay versus the LET of the striking particle.

and the particle energy. On the other hand, the device simulations are very time consuming. We performed Spice simulations in order to analyze induced soft delay due to these current pulses at the struck nodes of various gates. The gates were constructed in 100nm process technology with a V_{dd} of 1.2v. We used fan-out of two unit size inverters at the output of each gate. In Spice simulations, current pulses were injected during the signal transition at the gate output, typically when the signal is at $V_{dd}/2$. Figure 2 shows induced soft delay for three gates: NOT, NAND, and NOR. The y-axis depicts soft delay for various values of the particle LET of the x-axis. The amount of induced soft delay at a node depends on the striking particle LET, the total capacitance at the node, the driving strength of the transistor, and the V_{dd} value [7]. Also, the gate cell design has an impact on soft delays. It is clear from Figure 2 that the soft delay induced by even low energy particles ($\leq 5MeVcm^2/mg$) is quite large which is sufficient to cause a delay error in modern high speed circuits.

The soft delay at a node occurs regardless of the successful propagation to the circuit output. A Soft Delay Error (SDE) occurs when the propagation is not masked and the delayed signal is captured by the flip-flop(s) at the circuit output. The propagating soft delay can be masked by two effects:

Logic Masking: The soft delay will not propagate to the observable output of the circuit if there is no functionally sensitized logic path from the node to the observable output(s). A functionally sensitized logic path is the signal propagation path from a node to the circuit output(s) which is set by the state of the circuit inputs.

Timing Masking: The soft delay will not produce SDE if the affected signal (delayed signal) arrives earlier than the setup and hold time window the output flip-flop(s).

Note that, for the particle strike which produces a glitch, (i.e., SET), there is an additional masking effect called electrical masking which is due to the attenuation of the glitch [2], [3]. Since soft delay is not a glitch, electrical masking does not apply. If a signal is once delayed then it can propagate to the circuit output through functionally sensitized path(s) without attenuation of the delay.

In modern circuits, a guard band is introduced between the end of the critical path and start of the setup time as shown in Figure 3. The function of the guard band is to suppress cross talk induced pulses or other variations which can change, specifically increase the critical path delay. Signal (a) shows the transition arrival time during the normal (without particle strike) operations. Signal (b) depicts the

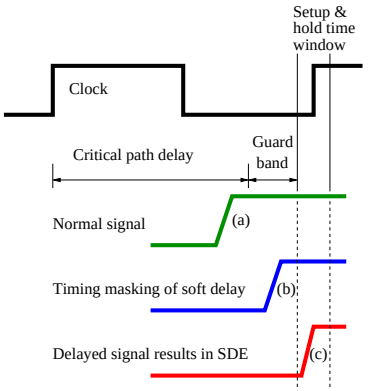

Fig. 3. Timing masking of the soft delay.

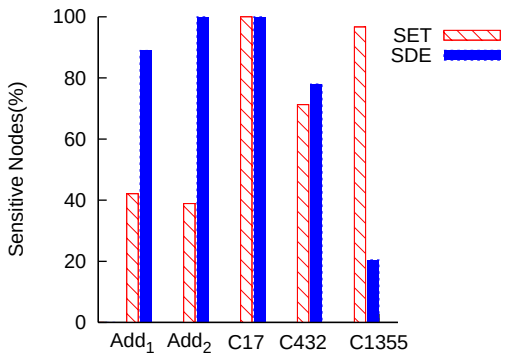

Fig. 4. The percentage of nodes sensitive to produce SDE and SET.

timing masking of soft delay i.e. the soft delay was suppressed by the guard band. The SDE occurs, as shown by signal (c), when the soft delay was sufficient to delay the signal beyond guard band.

B. Soft Delays and Glitches

The minimum (critical) soft delay, SD_{crit}, required at a node to produce a SDE depends on the transition occurrence time within the clock cycle and the path(s) delay from the node to the observable output(s). Figure 4 shows comparisons between the percentage of nodes sensitive to produce Soft Delay Errors (SDE) and Single Event Transients (SET), i.e. radiation-induced glitch errors, for the maximum LET = 20 $MeVcm^2/mg$. The data for SDE was obtained using our approach developed in section IV and for SET, we used an approach similar to approaches provided in [1], [2]. Circuits Add_1, Add_2, and $C17$ have critical path delay comparable to the soft delay produced by the particles of LET $\leq$ 20 $MeVcm^2/mg$. These circuits have higher percentage of sensitive nodes because particle strike at any node can produce sufficient delay to cause a SDE. The guard band used for these circuits was 20 ps. The main reason for SET less than SDE in some cases is due to radiation-induced glitch attenuation.

In Figure 4, we considered the sensitivity of a node to produce a SDE or SET based on the particle LET. However, the node sensitivity depends on additional factors as described in the following. In the case of SET, the node sensitivity concerns: 1) The critical energy of the particle. The critical energy is the minimum energy of the particle to produce a glitch which can propagate through the functionally sensitized path to the observable output(s) without significant attenuation such that when it arrives at the circuit output(s), it still has sufficient amplitude and width to be captured by the flip-flop(s). The critical energy is also used to determine the upset rate of the node. 2) The probability of the glitch propagation which depends on the state of the circuit inputs. 3) The timing window of vulnerability within a clock cycle i.e. the fraction of the clock cycle when the node is susceptible to produce a glitch which will arrive at the observable output during the setup and hold time window of the flip-flop(s).

Similarly, in the case of SDE, the node sensitivity concerns: 1) The critical energy of the particle. The critical energy is the minimum energy of the particle which produces sufficient delay such that the delayed signal arrives during or after the setup and hold time window. 2) The probability of the sensitive transitions. A sensitive transitions is a transition at a node which propagates to the circuit output and a particle strike on it can produce SDE. 3) The timing window of vulnerability within a clock cycle. The rise or fall time delay are the timing windows of vulnerability withing a clock cycle, these are the only timing windows during which a particle strike can produce soft delay.

As the clock rate keeps increasing, the probability of occurrence of SDE increases. Thus, in future technologies, at least where high reliability is required, the circuit failure due to SDE must be considered.

IV. Soft Delay Error Analysis Approach

We develop an approach for Soft Delay Error (SDE) analysis of transistor nodes of combinational circuits. In the following, we will analyze the sensitivity of a node to produce SDE and we will quantify it with a metric, S_{node}. A sensitive transition is a transition that results in SDE. The following aspects affect the node sensitivity, S_{node}: 1) The probability of sensitive transitions at the node. 2) The upset rate of the node which depends on the critical energy of the particle required to produce SDE. 3) The fraction of the transition delay time to the clock cycle. Note that a node is only sensitive to the particle strike to produce soft delay during the rising or falling transition. The node sensitivity metric, S_{node}, can be expressed as shown in equation (1):

$$S_{node} = P_{node} \times U_{node} \times T_{node} \quad (1)$$

Where P_{node} is the probability of the sensitive transitions at a node, U_{node} is the upset rate of the node, and T_{node} is the ratio of the transition delay to the clock cycle. In the following, we describe a methodology which is based on the steps of Figure 5 in order to determine U_{node}, P_{node}, and T_{node}.

Step 1 - *Cell library characterization for soft delay:* The main parameters to determine the amount of soft delay induced by a particle strike are: the striking particle energy (i.e., LET), the load capacitance at the node, the drive strength of the transistor(s) connected to the node, and the V_{dd} value. In this step, we will create several characterization tables using Spice for every gate of the cell library based on the LET and the load capacitance. For the given technology and cell library, these characterization tables are to be generated only once. This will allow us to eliminate time consuming Spice simulations of the circuit which otherwise would be used to obtain the critical energy of a particle at a node, $E_{node,gate}$. The $E_{node,gate}$ is required to determine U_{node}.

We characterize every sensitive transistor node in a gate based on equation (2).

$$D_{node,gate} = f_{node,gate}(E_{LET}, L_{out}) \quad (2)$$

where $D_{node,gate}$ is the soft delay produced at the output of the $gate$ by a particle strike at the $node$ and L_{out} is the capacitive load

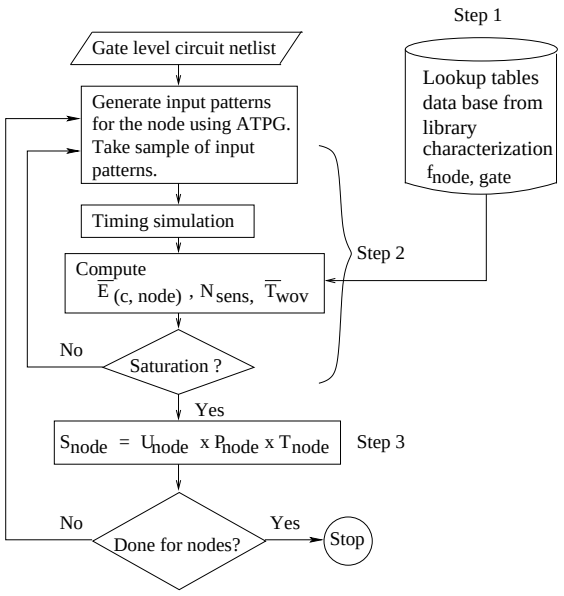

Fig. 5. Flow of SDE Analysis Approach.

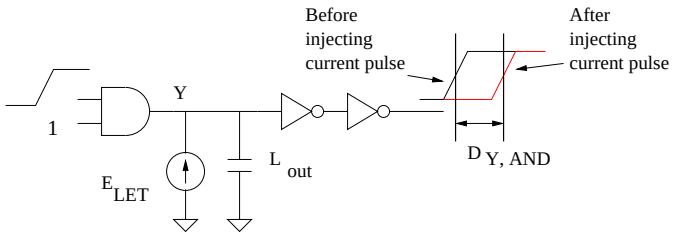

Fig. 6. Simulation setup for the characterization of an AND gate.

at the output of the gate. E_{LET} is the LET of the striking particle. The $D_{node,gate}$ under various values of L_{out} and the E_{LET} is recorded in a table.

Figure 6 depicts the simulation setup for the characterization of an AND gate. One input of the AND gate (the controlling input) is set to logic one while a rising transitions is applied at the other input. L_Y is the capacitive load at the output, Y, of the gate. A current source is connected between Y and Gnd to emulate the particle strike during the rising transition and between V_{dd} and Y for the falling transition. This current source is used to inject current pulses which were obtained for various values of the LET using device simulations as discussed in section III. Injecting a current pulse during the transition can distort it, we use two inverters in series to filter out the distortion. $D_{Y,AND}$ shows the soft delay which is the difference between the transition arrival time before and after injecting current pulses.

Table I shows an example of a characterization table of an AND gate of Figure 6. The second column shows the soft delay in pico-seconds for E_{LET} = 7 $MeVcm^2/mg$ under various values of L_Y of the first column. Similarly, the remaining columns show the soft delay for various values of E_{LET} and L_Y.

Step 2 - *Circuit node characterization:* In this step, we determine $E_{c,node}$, N_{sens}, and T_{wov} for every node of the circuit. $E_{c,node}$ is the critical (minimum) energy of a striking particle required at a node to produce a SDE. N_{sens} is the percentage of transitions at a node during which a particle strike results in a SDE. T_{wov} is the rise or fall transition delay time. This is the window of vulnerability (wov)

L_Y	E_{LET} $(MeVcm^2/mg)$			
	7	8	9	10
6 fF	60.60	79.70	93.00	100.80
8 fF	73.60	84.70	99.00	105.80
10 fF	78.60	89.70	104.00	110.80
12 fF	78.60	89.70	104.00	110.80

TABLE I
SOFT DELAY UNDER LOAD AND LET FOR AN AND GATE.

of a node to produce soft delay.

If the soft delay at a node of a gate, $D_{node,gate}$, and the load capacitance at the gate output, L_{out}, are known then the energy of a striking particle at a node can be determined using the inverse of equation (2) as shown in equation (3):

$$E_{LET} = f^{-1}_{node,gate}(D_{node,gate}, L_{out}) \quad (3)$$

E_{LET} of a gate node can be retrieved for given $D_{node,gate}$ and L_{out} by reverse lookup of the characterization tables. If $D_{node,gate}$ is the minimum delay required to produce a SDE then E_{LET} equals $E_{c,node}$, i.e. E_{LET} becomes the minimum energy of a particle required to produce $D_{node,gate}$ which is $E_{c,node}$. The L_{out} can be determined from the circuit layout. We perform timing simulations of the circuit for the sample of input patterns to determine $D_{node,gate}$. Note that Spice is not required to perform timing simulations, a logic level timing simulator can be used. An Automatic Test Pattern Generation (ATPG) tool is used to generated the input patterns for the circuit. Each pattern is a pair of input vectors. These patterns are applied to the circuit input in order to: 1) produce a signal transition at the node, 2) sensitize propagation path(s) from the node to the circuit output. During timing simulations of the circuit, we apply these patterns to the circuit inputs and record the transition arrival time at the primary output(s). Of course, there can be multiple paths from the node to the primary outputs and some paths might be converging. In this case, we consider the primary output which has the latest arrival time of the transition. The difference between the latest arrival time of signal transition during a clock cycle and the start of the setup time of the output flip-flop is $D_{node,gate}$ i.e. the minimum delay required to produce a SDE. The $D_{node,gate}$ varies with the transition occurrence time at the node and so does $E_{c,node}$.

We have found an interesting property of circuits that is when sample of input patterns are applied for a node of the circuit, the average of $E_{c,node}$, $\overline{E}_{c,node}$, saturates, meaning, it becomes stable within a small percentage of variation. Figure 7 shows $\overline{E}_{c,node}$ on the y-axis versus the number of transitions on the x-axis for the nodes of three different circuits. The top part of the figure shows the saturation of $\overline{E}_{c,node}$ for three different nodes of a four bit adder. Similarly, the middle and bottom parts of the figure show the saturation of $\overline{E}_{c,node}$ for the nodes of ISCAS85 benchmark circuits c432 and c1355.

During the timing simulations, if $E_{c,node} \leq E_{max}$ the transition is marked as sensitive otherwise insensitive, where E_{max} is the maximum energy of the striking, particle. We have also observed that the percentage of sensitive transitions, N_{sens}, at a node saturates. Figure 8 shows the saturation of N_{sens} at nodes of three different circuits. The x-axis depicts the number of transitions at the node and the y-axis depicts N_{sens}.

The procedure to determine $\overline{E}_{c,node}$, N_{sens}, and T_{wov} is as follows:

1) Take a sample of input patterns.

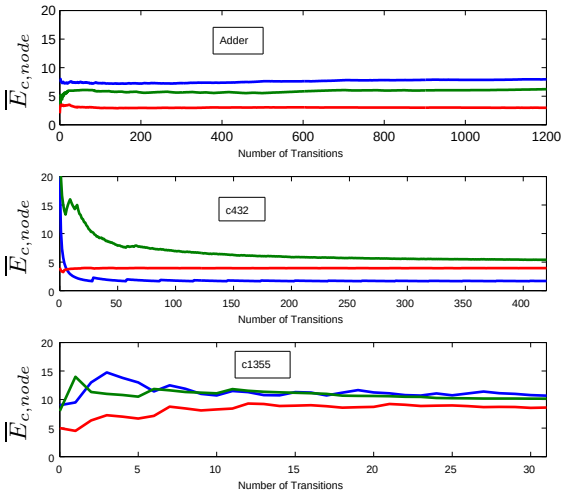

Fig. 7. Saturation of $\overline{E}_{c,node}$.

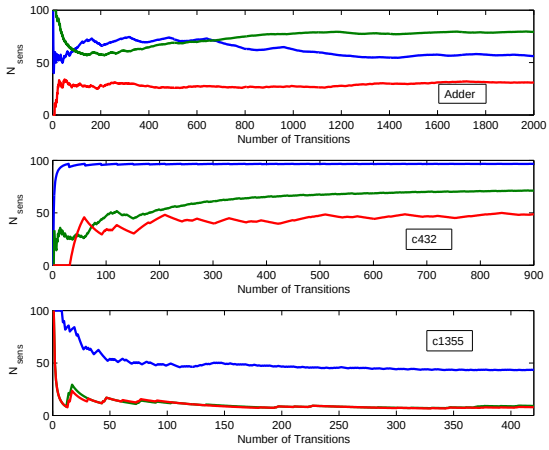

Fig. 8. Saturation of N_{sens}.

2) Generate $E_{c,node}$ for every pattern of the sample and mark the transition sensitive if $E_{c,node} \leq E_{max}$ otherwise insensitive. Also determine the transition delay time at the node, T_{wov}. The delay time for the rising transition is considered from 20% to 90% of V_{dd} and for the falling transition it is from 80% to 10% of V_{dd}.
3) For the taken sample, compute $\overline{E}_{c,node}$, the percentage of sensitive transitions (i.e., N_{sens}) and the average of T_{wov} (i.e., $\overline{T}_{wov}$).
4) Generate successive samples by incrementing their sizes.
5) Observation: when both the $\overline{E}_{c,node}$ and N_{sens} becomes stable within small percentage of variation, stop the timing simulations for the node.

Step3 - *Determining* S_{node}: Quantities U_{node}, P_{node}, and T_{node} of equation (1) are computed from $\overline{E}_{c,node}$, N_{sens}, and $\overline{T}_{wov}$, respectively. The U_{node} can be calculated using Neutron Cross-Section (NCS) approach proposed in [8] as shown in equation (4):

$$U_{node} = \int_{\overline{E}_{c,node}}^{E_{max}} \sigma_{nseu}(\overline{E}_{c,node}) \times (\frac{d\mathcal{N}}{dE})dE \qquad (4)$$

where $\sigma_{nseu}(\overline{E}_{c,node})$ is the neutron induced SEU cross-section which is the probability that a neutron of energy $\overline{E}_{c,node}$ can produce upset in a device in units of $cm^2/device$. The $\sigma_{nseu}(\overline{E}_{c,node})$ can be obtained from the layout of the logic circuit. $\frac{d\mathcal{N}}{dE}$ is the atmospheric differential neutron flux. We use an analytical approximation for $\frac{d\mathcal{N}}{dE}$ for New York City provided in [9] and [10].

The P_{node} is determined as shown in equation (5):

$$P_{node} = \frac{N_{sens}}{100 \times N_{Total}} \qquad (5)$$

Where N_{Total} is the total number of transitions at a node. Finally, the T_{node} is determined from equation (6):

$$T_{node} = \frac{\overline{T}_{wov}}{T_{cycle}} \qquad (6)$$

Where T_{cycle} is the clock cycle time of the circuit.

V. Results and Discussion

The node sensitivity analysis approach for soft delay errors described in section IV was implemented in PERL and C. Using this approach, we calculated the node sensitivity of two ISCAS85 circuits and two adders. All the circuits were implemented in 100nm process technology using scaled MOSIS layout design rules. The Spice parameters were obtained from [15], [16] and the supply voltage for these circuits was 1.2v.

In order to compare the simulation (run) time and accuracy between our approach and Spice, we performed node sensitivity analysis of two 4 bit adders and an ISCAS85 circuit (c17). These simulations were performed on Sun Blade 1000 workstation running Solaris 9. Adders, Add_1 and Add_2 have similar structure to 74283 and 74182 circuits. Table II shows the run time and accuracy comparisons between Spice simulations, t_{Spice}, and our approach, t_{SDEA}. The second column shows the number of nodes analyzed for the circuits of first column. We observed that the accuracy of our approach is close (less than 5% error) to Spice while it is orders of magnitude faster than Spice. Spice based analysis is very time consuming because it is performed in nested loops. For example, for the complete analysis of N nodes in a circuit with I inputs and E particle energy levels, we have to perform $N \times (2^{2I} - 2I) \times E$ simulations [11]. The term $2^{2I} - 2I$ ensures all the possible transitions at a node. It is clear from table that our approach can be used to analyze large circuit like c432 and c1355 which have large number of inputs and gates. It is not feasible to perform Spice analysis for these circuits.

Circuit	Nodes	t_{Spice} (min)	t_{SDEA} (min)	Speedup	Relative (% Error)
Add_1	38	25900	1.16	2.23× 10^4	4.11%
Add_2	19	14100	0.55	2.5× 10^4	3.28%
$c17$	6	1900	0.16	1.1×10^4	5.00%
$c432$	161	Not feasible	8	-	-
$c1355$	546	Not feasible	110	-	-

TABLE II
Accuracy and run time comparisons.

Table III shows the normalized node sensitivity, S_{node}, of various ISCAS85 circuits and two adders (Add_1 and Add_2). The node sensitivity of a node in the circuit is normalized with respect to the node with the largest sensitivity. The first column shows normalized sensitivity range and the remaining columns show the percentage of nodes of every circuit which comes in normalized sensitivity range of the first column. The bottom two rows show the number of analyzed nodes and the number of primary inputs (PIs) for every circuit.

S_{node}	c1355	c432	c17	Add_1	Add_2
0	72%	22%	0	11%	0
≤ 0.1	24%	35%	0	45%	63%
≤ 0.2	4%	12%	0	21%	32%
≤ 0.3	0	2%	0	13%	5%
≤ 0.4	0	4%	0	2%	0
≤ 0.5	0	7%	0	2%	0
≤ 0.6	0	6%	0	5%	0
≤ 0.7	0	3%	16%	0	0
≤ 0.8	0	5%	0	0	0
≤ 0.9	0	2%	50%	0	0
≤ 1	0	2%	34%	0	0
Analyzed nodes	546	161	6	38	19
Number of PIs	41	36	5	9	9

TABLE III
NORMALIZED SENSITIVITY OF NODES.

It is clear from Table III that the sensitivity of the nodes in circuit is not uniformly distributed which is similar to remarks in [1], [2]. The Soft Error Rate of a circuit can be reduced by reducing the sensitivity of highly sensitive nodes. One of the techniques to reduce the node sensitivity is node hardening techniques [13], [17].

We used an electrical node hardening technique to reduce the node sensitivity of example circuits - Add_1 and Add_2. This node hardening technique is based on changing (increasing) the size of transistors connected to the node. The total number of nodes in Add_1 and Add_2 are 36 and 19, respectively. We applied hardening on only six highly sensitive nodes of each circuit. In this case, the size of transistors, which are connected to the selected node, was arbitrarily increased by 2 times. Table IV shows reduction in total sensitivity of Add_1 and Add_2 before and after applying the hardening technique. The fourth column shows the total sensitivity reduction in Add_1 is 69% and in Add_2 is 30% while circuit area increase (shown in fifth column) for Add_1 and Add_2 is 17% and 26%, respectively. It is clear from Table IV that the soft error rate of the circuit can be dramatically reduced by applying node hardening techniques on the selected nodes with a small percentage of the circuit area increase.

Circuit	Total sensitivity		Sensitivity reduction	Area increase
	Before Hardening	After Hardening		
Add_1	4.82	1.49	69%	17%
Add_2	1.67	1.17	30%	26%

TABLE IV
REDUCTION IN THE CIRCUIT SENSITIVITY AFTER APPLYING NODE HARDENING TECHNIQUE.

VI. CONCLUSION

We introduced the notion of Soft Delay Error (SDE) analysis of CMOS circuits. We proposed an analysis approach for the node sensitivity to SDE effects. We performed mixed-mode simulation to extract current pulses for the characterization of SDE. We defined a node sensitivity metric and a step by step procedure to compute it. The further key contribution are: 1) a technique for logic cell library characterization based on lookup tables to determine critical energy of the particle. The lookup table technique avoids time consuming Spice simulations which otherwise should be used to compute the critical energy of the particle. 2) Deriving a fast saturating averaging of the critical energy of the particle which helps to reduce the simulation time. 3) Deriving a fast saturating averaging of the percentage of sensitive transitions which reduces simulation time by reducing the test set to compute the probability of sensitive transitions.

Using this approach, we provided distributions of sensitivity of nodes for various ISCAS85 circuits. Our approach is orders of magnitude faster than Spice based analysis techniques with accuracy close to Spice. This approach is complementary to the glitch analysis approach in the sense that they both provide comprehensive reliability analysis of CMOS circuits. By analyzing and determining the nodes sensitivity to SDE, node harding techniques can be applied to protect selected highly sensitive nodes. This is demonstrated for two test circuits.

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