SRAM Cell Design Using Tri-state Devices for SEU Protection

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Abstract. A new SRAM cell model, SRAMT, is presented providing a scalable solution to soft error for various energy levels of protection with minimal power consumption and write time penalties. Our model is based on a classic 6 transistor inner core SRAM cell and an outer core consisting of enhanced tri-state inverters. The outer core will absorb a particle strike at a sensitive node of the SRAM cell without a major impact on write time performance or area overhead. The model provides an on-demand protection due to the fact that the outer core can be shut off during non-essential operating mode. The on-demand aspect of the design provides a much more favorable power consumption overhead compared to the existing protection techniques. We simulated extensively our model and provided results for various energy levels of soft error protection as well as layout area, performance and power consumption overhead in comparisons to hardened standard memory cells.

1 Introduction

In today's microprocessors, embedded memories occupy more than 30% of the chip area and in SoCs they may exceed 60% . However, as technology scales down and the supply voltage decreases memories are becoming more prone to reliability problems. One of the main reliability concerns comes from particle strikes that create SEUs (single event upsets) in memories. This is a major problem in mission critical applications where reliability is a main concern on a par with performance and cost. In past technologies, this problem was significant in radiation hostile environments such as in space. However, very-deep-submicron technologies with aggressive device and voltage supply downsizing have significantly reduced the critical charge of memory cells. This means low energy particles can flip memory cells, making memories sensitive to atmospheric neutrons as well as to alpha particles created from materials within the chip. In addition, the increased number and density of cells leads to increased probability of SEU occurrence [1, 2, 3, 4, 5].

Soft errors and SEUs indicate the same phenomenon, namely a bit flip caused by an energetic particle hit generating a charge that, if collected by sensitive regions of the circuit, can temporarily alter the logic value in that node. In a regenerative circuit, such as a SRAM cell, this temporary voltage glitch can be fed back and thus confirmed as a bit flip. Thus SEUs may manifest as errors when the collected charge Q at that particular node exceeds some critical value and results in logic state changes for storage elements such as memory, latches and registers. In addition, the increased number and density of nodes leads to increased probability of soft errors.

Therefore, the increased sensitivity of SRAM to soft errors is a major reliability issue for modern CMOS technology even at the ground level. Current research suggests that the average rate of failure for complex chips may be in excess of four errors per year [15].

There have been many solutions to create a soft error immune SRAM cell. These solutions can be broken down into three categories: a) hardening, b) recovery, c) protection. Hardening techniques insert circuitry in an SRAM cell possibly duplicating the number of transistors [6, 7]. Recovery techniques insert current monitors in SRAMs to detect SEUs and they employ error correcting codes or redundancy to mitigate these effects [8]. These techniques do not scale very well. Protection methods use capacitors in SRAM cells to absorb the excessive charge [15, 16, 17]. Although they provide sufficient protection, they adversely affect the cell performance. Another drawback to the capacitive based solution is the area overhead.

In this paper we explore some of the existing protection techniques as well as propose a new non-capacitive based protection mechanism for an SRAM cell. We address performance drawbacks of the existing techniques as well as the area concerns in our proposed SRAM design. The major contribution of this paper is a new SRAM cell design, labeled "SRAMT" which provides increased level of protection compared to the standard SRAM cell, while minimizing the power consumption

and write time performance penalty. The model provides an on-demand protection due to the fact that the outer core can be shut off during non-essential operating mode. We support our proposed design with various Hspice models and simulations for various energy levels of soft error protection. This paper is organized as follows. In section 2, we discuss the background of soft errors in SRAM cells. In section 3, we discuss our approach to a protected SRAM cell design based on tri-state device. In section 4, we describe the simulation and results for our proposed SRAM cell design. The conclusion is in section 5.

2 Background

A Single Event Upset (SEU) in the SRAM occurs when a charged particle strikes a sensitive node and flips the state of the SRAM cell from 0 to 1, and vice versa, causing a soft error. This is temporary, i.e. the cell is not permanently damaged and it can be rewritten in the next memory write cycle, nonetheless if the flipped cell is read out the error value may cause a system failure.

Every memory cell has two sensitive nodes, i.e. the drains of the OFF-NMOS and of the OFF-PMOS transistors, respectively. The drain and substrate of the OFF-transistor create a reverse-biased junction. The reverse-biased junctions of the cell are most sensitive nodes to the particle strike. Immediately after a particle strike, the generated charges are collected at the opposite voltage terminals of the reverse-biased junction, meaning electrons and holes move towards the positive and negative voltage, respectively. The movement of charges cause a current pulse with width of few hundred pico-seconds. The memory cell flips when the collected charge, Q, is larger than the stored charge at the struck node. The minimum charge required to flip the cell is called Q_{crit}. The Q_{crit} not only depends on the collected charge but also on the shape of the current pulse [6, 9, 10, 11, 12], as well as the strength of the gate driving the node. A 1 to 0 flip occurs when a particle strike discharges the charge stored at the drain of the OFF-NMOS transistor, and similarly, a 0 to 1 flip occurs when a particle strikes at the drain of the OFF-PMOS transistor. As technology scales down, the charge stored at the sensitive nodes of the memory cell is reduced because $Q_{node} = C_{node} \times V_{dd}$ making SRAM more prone to soft errors.

A standard 6-transistor SRAM cell is shown in Fig.1. For convenience in the discussion to follow, Fig 1 is abstracted into the block cell structure of Fig. 2. Nodes Q and $\bar{Q}$, store the information in the cell. This information is read out and written to by the bitlines, BL and $\overline{BL}$, respectively. The state of the SRAM cell is determined by the word line, WL. When the word line is active, the cell is in write/read mode and when the word line is in-active the cell is idle or in "standby" mode. The standby mode is considered to be most vulnerable to a SEU. Thus most protection techniques are focused on protecting the SRAM cell during its standby mode.

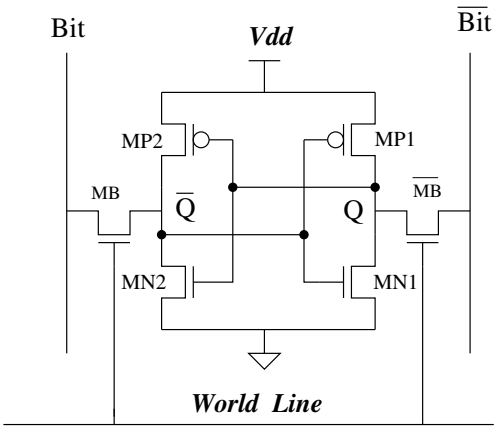


Figure 1. Standard SRAM cell

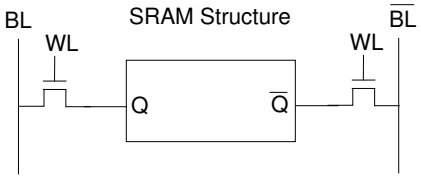
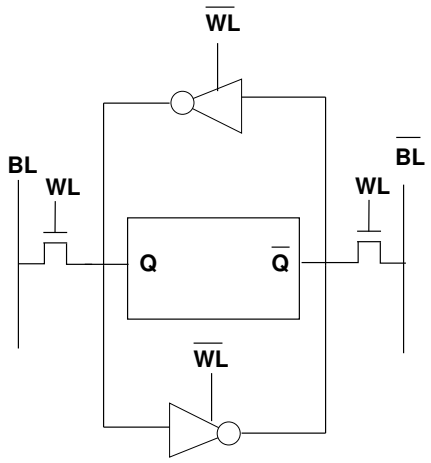


Figure 2. SRAM block

A major characteristic of the capacitive-based protection models involves creating charge buffer nodes, i.e. capacitors, that are connected to the SRAM cell. The capacitors create buffers between the Q and $\bar{Q}$ nodes, such that even if a SEU happens at one of these nodes the cell state is not affected, as the potential difference between and nodes remains the same. One such model was pioneered in [18] with the capacitors vertically stacked above the SRAM cells, to minimize the footprint. The major weakness of all the models is the fact that the capacitor nodes adversely affect the write time it takes for a system to switch states during a write mode which also affects the performance of the cell. There are protection models that do not use capacitors but on the other hand try to lock the SRAM cell information by disconnecting some of its components. One of such models has been presents in [19], however such approach is very application specific and does not deliver total SEU protection.



SRAM Cell with Tri–State Inverters

Figure 3. Modified SRAM cell – SRAMT

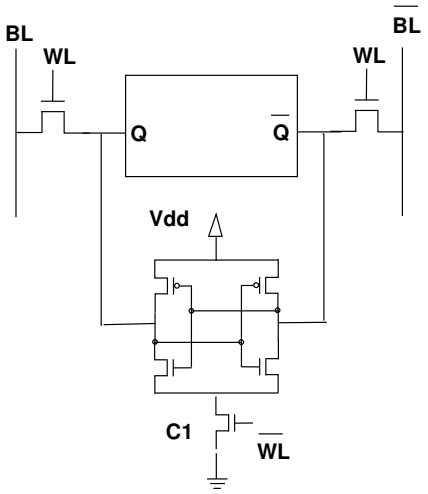
3 Approach

As we mentioned before, the addition of any extra components to the SRAM circuit creates performances drawbacks. The system takes more time to change states and thus the performance of the cell suffers. The immediate response to such a problem is to make the additional components dynamic and only available when they are required.

Our proposed SRAMT model consists of a regular SRAM cell with an addition two tri-state inverters that are connected to the WL and $\overline{WL}$ as can be seen in Figure 3. The two tri-state inverters are classified as the outer core of the SRAM while the original cell is classified as the inner core.

During a standby mode the outer core tri-state inverters are used to strengthen the charge value of the inner core cell, which has the effect of increasing the critical charge at the nodes, Q and $\bar{Q}$,. With an addition of the outer core elements the tolerance level of the SRAM cell to SEUs is greatly improved. The level of tolerance is dependent on the physical parameters and characteristics of the transistors in the outer core inverters. Furthermore, during the write mode the outer core tri-state inverters are turned off. Thus only the inner core of the SRAM cell is active during the write mode and the write performance is only minimally affected. The turned off tri-state inverters introduce some minor input gate capacitance, which impacts the write time. Once the write mode is completed, the outer core is activated once again and the signal value in the SRAM cell is strengthened.

One of the concerns about the SRAMT cell design shown in Figure 3 is the area overhead. Each of the tri-state inverters in the outer core of the cell consists of 4 transistors. Such a tri-state inverter design, brings the total number of transistors of the newly proposed SRAMT cell to 14. The total transistor count overhead of SRAMT cell is 133% of the standard 6 transistor SRAM cell. In order to reduce the transistor count overhead, we propose to redesign the tri-state inverter for the outer core of the SRAM cell. The new design can be seen in Figure 4. The tri-state inverter design, SRAMT, is reduced from 4 transistors to 2 transistors plus a control transistor that is shared by both inverters. The shared transistor labeled C1 in Figure 4 turns the tri-state inverters off during the write mode and back on during the standby mode. Finally, the actual physical layout overhead will be discussed in the next section.



SRAM Protected

Figure 4. Final SRAMT Design

In all the previous figures and designs, we assumed that the outer core and the inner core transistors have the same physical characteristics and parameters. However, the level of tolerance to SEU is dependent on the physical characteristics of both inner and outer cores of the SRAMT cell. In order to raise the tolerance levels we increased the width of each of the transistors in the outer core design to boost the drive strength of the outer core, while the inner core transistors remain the same. By doing so, we strengthen the charge value of the tri-state inverters and increased the protection level of the cell. However, there are drawbacks for raising the level of SEU protection in such fashion. The layout area overhead, power consumption overhead and write time performance are effected by this change. We investigate the effect strengthening of the new SRAMT has on area, performance and power in HSpice. We compare our results to existing protection techniques such

as hardening of the original SRAM cell, which we also simulate in HSpice.

4 Simulations

In our simulations we first find the corresponding relationship for similar levels of protections between our proposed designs and existing protection techniques such as transistor hardening. Using this corresponding relationship we compare the characteristics of each circuit in regards to area, performance, power consumption: for area, we used physical layout comparison; for performance, we compared the write time delay of the cells during a write operation; for power, we measured the average and the peak power consumption during a write operation. The idea behind this method is to show that while providing the same levels of soft error protection, our novel design excels in other circuit characteristics compared to other protection techniques.

In order to perform all of our simulations we designed seven SRAM cell models. The first design cell is a standard 6-transistor SRAM, SRAM1x Fig. 1, we use this cell model as a benchmark for all characteristic comparisons. The next three SRAM models are hardened SRAM cells, by resizing the inverter transistors widths appropriately: SRAM2x, SRAM3x, SRAM4x. The inner core transistors are hardened 2x, 3x and 4x respectively. The last three cell models are the proposed cell models shown in Fig.4 - SRAMT1x, SRAMT2x, SRAMT3x. The major difference between these three cells is the fact that for SRAM2x and SRAM3x the outer core transistors are hardened 2x and 3x respectively, while the inner core transistors are left unchanged for all SRAMT cells. These cells are designed using 100nm process technology. The power supply voltage, V_{dd} for this technology was used as 1.2v, while the HSpice parameters were obtained from Predictive Berkeley technology data [13]. All layout designs were made using Electric tools [20]. The layouts for the SRAMT designs were heavily optimized for maximum area reduction.

To determine the various levels of protections for all SRAM cells, we simulated SEU upsets in all of our designs. In the following simulations, a particle strike is modeled by injecting a current pulse at the sensitive node [14]. The pulse has a rather rapid rise time and a gradual fall time. The shape of the pulse can be approximated by the following equation:

$$I(t) = \frac{2Q}{\sqrt{\pi}} \times \sqrt{\frac{t}{T}} \times e^{\frac{-t}{T}}$$

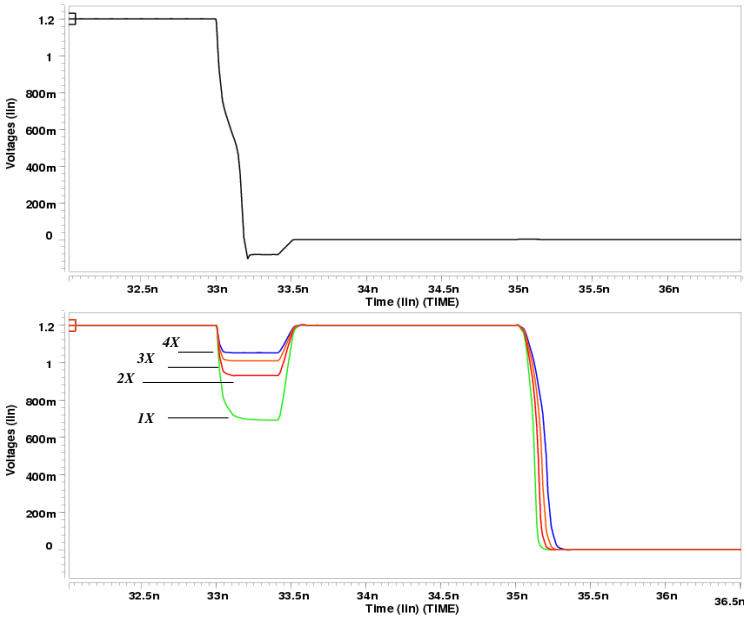


Figure 5. combined SEU recovery results for 1 cycle

Where Q is the charge collected due to the particle strike and T is the process technology constant. To demonstrate the new SRAMT behavior to SEU, we injected a current pulse into the original SRAM1 cell and to the three SRAMT cells, SRAMT1x, SRAMT2x, SRAMT3x. The energy level of the injection was kept the same for all four cells to demonstrate the collapse of the normal SRAM cell and the recovery levels of the new SRAMT cells with different drive strengths. Figure 5 shows the results of the injection simulations for all four cells. The top graph represents the original SRAM cell, while the bottom graph in Figure 5 represents four new SRAMT cells. The logical bit value corresponds to the voltage probing of a node Q in all cells. A particle strike is injected at 33ns mark into all cells. The original cell collapses and results in a bit switch as the logical value goes from 1 to 0. However, the new SRAMT cells recover from the simulated particle strike. The recovery process directly relates to the drive strength of the SRAMT. The 1X drive strength SRAMT cell is affected much more then 2X drive strength SRAMT cell by the particle strike. This behavior is expected as the tolerance level of the 2X drive strength SRAMT is higher then 1X due to physical characteristics. Furthermore, it is clear from Figure 5 that each of the new SRAMT cells has a different critical charge, Q_{crit}, value.

In order to determine Q_{crit} of a cell node, we performed HSpice simulations by injecting current pulses of equation above for various values of Q. The minimum values of Q which results in a cell flip is considered as Qcrit of that node. We produced Q_{crit} values

for all five SRAM models. In order to perform a logical 0 to logical 1 switch, a lot more energy is required than for a logical 1 to logical 0 switch. Thus the cell is more vulnerable to a 1 to 0 flip. We also ran the same type of simulations on resized cell models: SRAM2x, SRAM3x and SRAM4x. The Table 1 demonstrates the critical charge for a 1 to 0 flip for all of the seven SRAM cell models.

The results from Table 1 show that SRAMT1x has almost identical critical charge Q_{crit} as SRAM2x, the same holds true for SRAMT2x versus SRAM3x and SRAMT3x versus SRAM4x. Thus the following pairings give the same level of SEU protection: SRAMT1x and SRAM2x, SRAMT2x and SRAM3x, SRAMT3x and SRAM4x. Having determined the equivalence between existing and proposed protection technique, we compared the techniques in area, performance and power consumption.

CRITICAL CHARGE

SRAM cells			Tri-state cells		
Cell	Carge	%	Charge	%	Cell
2X	19.2fC	100%	19.8fC	106%	T1X
3X	29.0fC	202%	29.6fC	208%	T2X
4X	40.2fC	318%	39.4fC	310%	T3X

Table 1. Critical Charge and Extra charge protection improvement (in %) of a) hardened SRAM cells and b) tri-state cells in reference to a standard SRAM cell critical charge of 9.6fC

Table 2 gives the additional layout area overhead in percentage compared to the standard SRAM1x cell. The additional transistors incurred by the tri-state design in SRAMT cells result in a maximum of 5% addition overhead to hardened SRAM cells.

LAYOUT AREA

SRAM cells		Tri-state cells	
Cell	Extra area	Extra area	Cell
2X	32.9%	37.7%	T1X
3X	68.1%	73.3%	T2X
4X	88.3%	89.6%	T3X

Table 2. Layout area overhead (in %) required for a) hardened SRAM cells and b) tri-state cells in reference to a standard SRAM cell

We begin our model design versus write time performance experiments by observing the bit write operation for a value of 1 in all SRAM cells. The new value of 1 is written over the the previous value of 0 at 25ns mark. The logical bit value corresponds to the voltage probing of a node Q. Each of the cell designs have a different effect on the write time delay during the write operation, we compile the write delay data in Table 3.

Clearly Table 3 shows a trend of improvement of write time performance of the SRAMT cells over the hardened SRAM cells.

WRITE TIME

SRAM cells			Tri-state cells		
Cell	Time	%	Time	%	Cell
2X	.162ns	17.4%	.161ns	16.7%	T1X
3X	.186ns	34.7%	.181ns	31.1%	T2X
4X	.227ns	64.5%	.203ns	47.1%	T3X

Table 3. WRITE time and Time Overhead (in %) required by a) hardened SRAM cells and b) tri-state cells in reference to a standard SRAM cell WRITE Time 0.138ns

In the next set of experiments we investigate power consumption of each of the protection models. We probe both the average power and the peak power, we compare the power overhead to the standard SRAM1x cell for all six protection models. The data for average power is compiled in Table 4.

Table 4 shows that in each case for the SRAMT design there is a clear improvement in average power (AV) consumption overhead over the hardened cells. A similar improvement is shown in Table 5 for peak power overhead data. One of the features of the SRAMT design is the ability to reduce the peak power since the tri-state inverters are not active during the write operation, i.e. WL is active. Furthermore, we can see that there is a trend of the average power overhead for the hardened design getting ever increasingly worse compared to the SRAMT design. Peak power is an important consideration in overloading metal layers in sub-micron design.

5 Conclusion

In this paper we provided a novel approach to soft error protection techniques for SRAM cell, SRAMT. Our model is based on a classic 6 transistor inner core SRAM cell and an outer core consisting of enhanced

AV POWER

SRAM cells		Tri-state cells	
Cell	Extra AV Power	Extra AV Power	Cell
2X	133%	119%	T1X
3X	315%	235%	T2X
4X	587%	366%	T3X

Table 4. Extra Average Power overhead required (in by a) hardened SRAM cells and b) tri-state cells in reference to a standard SRAM cell AV Power of $2.53 \times 10^{-5}w$

PEAK POWER

SRAM cells		Tri-state cells	
Cell	Extra Peak Power	Extra Peak Power	Cell
2X	131%	108%	T1X
3X	240%	170%	T2X
4X	301%	223%	T3X

Table 5. Extra Peak Power overhead required by a) hardened SRAM cells and b) tri-state cells in reference to a standard SRAM cell, peak Power $1.17 \times 10^{-4}w$

tri-state inverters. We demonstrated how the design of our SRAMT cell provides advantages in terms of performance and power consumption overhead compared to the existing soft error protection techniques through transistor hardening. Through simulations we were able to demonstrate that our new design provides identical energy levels of protection to the existing protection techniques at minimal area overhead, while providing advantages in write time delay performance and great reduction in power consumption for both average power and peak power during write time operation. Our solution is also technology scalable, which is especially crucial for submicron designs.

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