SRAM cell design protected from SEU upsets

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• ***Abstract***. In this paper we present a new SRAM model which provides protection of memories from soft errors. Our model is based on a combination of a capacitor and CMOs transistors which can absorb the excess SEU charge that may strike a sensitive node of the SRAM cell. At the same time, our design technique does not affect the normal memory cycle time. This is in contrast to other capacitive based memory protection models which adversely affect the normal memory write time. We simulated extensively our model in HSPICE, and provide experimental results and comparisons.

1 Introduction

In today's microprocessors, embedded memories occupy more than 30% of the chip area and in SoCs they may exceed 60% . However, as technology scales down and the supply voltage decreases memories are becoming more prone to reliability problems. One of the main reliability concerns comes from particle strikes that create SEUs (single event upsets) in memories. This is a major problem in mission critical applications where reliability is a main concern on a par with performance and cost. In past technologies, this problem was significant in radiation hostile environments like in space. However, very-deep-submicron technologies with aggressive device and voltage supply downsizing have reduced significantly the critical charge of memory cells. This means low energy particles can flip memory cells, making memories sensitive to atmospheric neutrons as well as to alpha particles created from materials within the chip. In addition, increased number and density of of cells leads in increased probability of SEU occurrence [1, 2, 3, 4, 5].

Soft errors are caused by SEUs carrying excess charge that results in flipping a bit in a SRAM. Thus SEUs may manifest as a soft error when the collected charge Q at that particular node exceeds some critical value and results in logic state changes for storage elements such as memory, latches and registers. In addition, increased number and density of nodes leads in increased probability of soft errors.

Therefore, increased sensitivity of SRAM to soft errors is a major reliability issue for modern CMOS technology even at the ground level. Current research suggests that the average rate of failure for complex chips may be in excess of four errors per year [15].

There have been many solutions to create a soft error immune SRAM cell. These solutions can be broken down into three categories: a) hardening, b) recovery, c) protection. Hardening techniques insert circuitry in an SRAM cell possibly duplicating the number of transistors [6, 7]. Recovery techniques insert current monitors in SRAMs to detect SEUs and they employ error correcting codes or redundancy to mitigate these effects [8]. These techniques do not scale very well. Protection methods use capacitors in SRAM cells to absorb the excessive charge [15, 16, 17]. Although they provide sufficient protection, they affect adversely the cell performance.

In this paper will concentrate on some of the existing protection techniques as well as propose a new protection mechanism for an SRAM cell. We address these performance drawbacks of the previous techniques in our proposed SRAM design.

The major contribution of this paper is a new SRAM cell design, labeled " SRAM-tct", which maintains the protection level of capacitive-based techniques while retaining the performance level of a regular SRAM cell. We support our proposed design with various hspice models and simulations and comparisons to existing memory protection methods.

2 Background

A Single Event Upset (SEU) in the SRAM occurs when a charged particle strikes a sensitive node and flips the state of the SRAM cell from 0 to 1, and vice versa, causing a soft error. This is temporary, i.e. the cell is not permanently damaged and it can be rewritten in the next memory write cycle, nonetheless if the flipped cell is read out the error value may cause a sys-

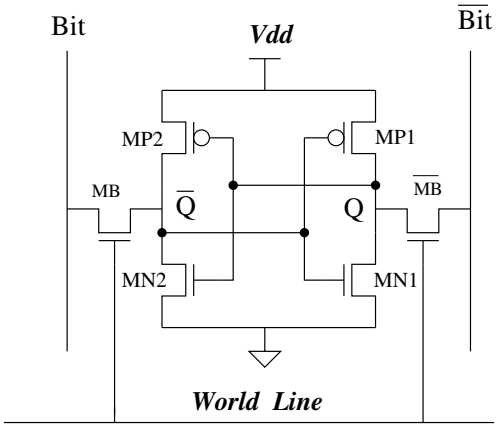

Figure 1. Standard SRAM cell

tem failure.

Every memory cell has two sensitive nodes, i.e. the drains of the OFF-NMOS and of the OFF-PMOS transistors, respectively. The drain and substrate of the OFF-transistor create a reverse-biased junction. The reverse-biased junctions of the cell are most sensitive nodes to the particle strike. Immediately after a particle strike, the generated charges are collected at the opposite voltage terminals of the reverse-biased junction, meaning electrons and holes move towards the positive and negative voltage, respectively. The movement of charges cause a current pulse with width of few hundred pico-seconds. The memory cell flips when the collected charge, Q, is larger than the stored charge at the struck node. The minimum charge required to flip the cell is called Q_{crit}. The Q_{crit} not only depends on the collected charge but also on the shape of the current pulse [6, 9, 10, 11, 12]. A 1 to 0 flip occurs when a particle strike discharges the charge stored at the drain of the OFF-NMOS transistor, and similarly, a 0 to 1 flip occurs when a particle strikes at the drain of the OFF-PMOS transistor. As technology scales down, the charge stored at the sensitive nodes of the memory cell is reduced because $Q_{node} = C_{node} \times V_{dd}$ making SRAM more prone to soft errors.

A standard 6-transistor SRAM cell is shown in Fig.1. For convenience in the discussion to follow, Fig 1 is abstracted into the block cell structure of Fig. 2. Nodes Q and $\bar{Q}$, store the information in the cell. This information is read out and written to by the bitlines, BL and $\bar{BL}$, respectively. The state of the SRAM cell is determined by the word line, WL. When the word line is active, the cell is in write/read mode and when the word line is in-active the cell is idle or in "standby" mode. The standby mode is considered to be most vulnerable to a SEU. Thus most protection techniques are focused on protecting the SRAM cell during its standby mode.

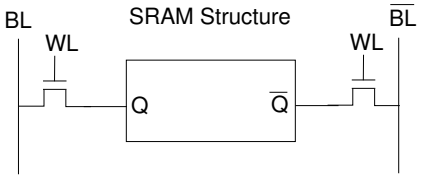

Figure 2. SRAM block

• **Capacitive based models**. A major characteristic of the capacitive-based protection models involves creating charge buffer nodes, i.e. capacitors, that are connected to the SRAM cell. The placements of the capacitors in the SRAM cell differs from model to model, however, the idea behind using the capacitors is basically the same. The capacitors create buffers between the Q and $\bar{Q}$ nodes, such that even if a SEU happens at one of these nodes the cell state is not affected, as the potential difference between and nodes remains the same. One of such models, labeled SRAMc2, is shown in Fig 3. This model was pioneered in [18] with the capacitors vertically stacked above the SRAM cells, to minimize the footprint.

The SEU charge tolerance of the SRAMc2 is dictated by the size of the capacitors used. High capacitance will result in high charge tolerance levels. As we mentioned before there are other placement models for capacitor nodes as can be seen in figure 4. This was suggested in [16, 17]. The idea behind these capacitor models can be summarized by an equivalent circuit shown in Figure 5.

The major weakness of all the models summarized by SRAM-c is the fact that the introduction of the capacitor nodes greatly affects the time it takes for a system to switch states during a write mode. The write time decrease directly affects the performance of the cell. Thus while the SRAM-c design creates an SEU protection threshold, the cell immunity comes at the price of the performance. There are protection models that do not use capacitors but on the other hand try to lock the SRAM cell information by disconnecting some of its components. One of such models has been

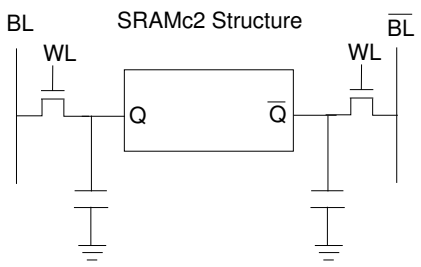

Figure 3. Modified SRAM cell – SRAMc2

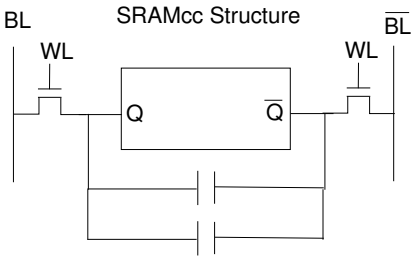

Figure 4. Modified SRAM cell – SRAMcc

presents in [19], however such approach is very application specific and does not deliver total SEU protection. We propose an SRAM design that exhibits the

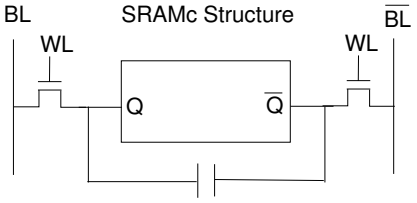

Figure 5. Modified SRAM cell – SRAMc

protection qualities of the SRAM-c but without the performance penalty.

3 Approach

As we mentioned before, the addition of any extra components to the SRAM circuit creates performances drawbacks. The system takes more time to change states and thus the performance of the cell suffers. The immediate response to such problem is to make the additional components dynamic and the only available when they are required.

Our proposed model consists of a regular SRAM cell with an addition of two CMOS transistors connected in series with two NMOS transistors and a vertically stacked capacitor as shown in Figure 6. The PMOS transistors are connected to the $\bar{W}L$ and WL respectively. The PMOS transistors act as switches to turn on and off the capacitor. The NMOS transistors that are connected to the WL are used to discharge the capacitor during a write phase when word line is high. During a standby mode the capacitor is connected to the SRAM cell and acts as a charge buffer. When a write mode is activated, the PMOS switch transistors detach the capacitor from the SRAM. Then the NMOS transistors connect to GND and completely discharge the capacitor. Once the write phase is finished the capacitor is re-introduced into the system. The charge on the capacitor is reflective of the current system state and will take some time to aquire. Once the SRAM cell and the capacitor sync the capacitor continues to act as a charge buffer in case of a SEU.

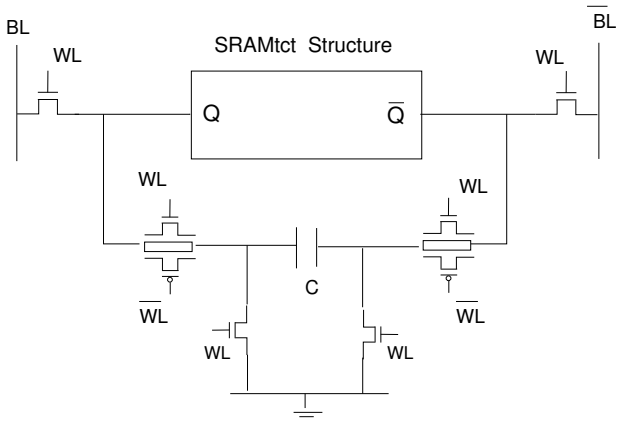

Figure 6. Modified SRAM cell – SRAMtct

We focus our attention on the write performance of this model, the amount of time it takes to switch logical values. We also focus on the tolerance levels of the proposed model vs existing models. We compare our model to regular SRAM and SRAM-c models in order to validate our assumption that the proposed model exhibits excellent performances while maintaining equal protection to other capacitor based models. We run multiple experiments in HSpice to validate our proposal.

4 Simulations

In our simulations we run two types of experiments, the first bulk of experiments concentrates on the relationship between capacitance and write time performance of various model cells. We monitor the amount of time it takes to write a new value into a selected node and track how this value changes as we introduce more capacitance to the SRAM models. In the second bulk of the experiments we focus on the relationship between critical charge and capacitance of various models. We simulate a particle strike by injecting a current pulse at the sensitive node for each SRAM model. We then observe the effect of various capacitance of each model to the system behavior post injection period.

In order to perform both type of the experiments we designed three cell models. These three cells are: standard 6-transistor SRAM, Fig. 1, SRAM cell with a capacitor, SRAM-c Fig. 5, SRAM cell with a two CMOS transistors, two PMOS transistors and a capacitor, SRAM-tct shown in Fig. 6. These cells are designed in 100nm process technology. The power supply voltage for this technology was used as 1.2v and the HSpice parameters were obtained from Predictive Berkeley technology data [13].

For individual cell construction, we build the transis-

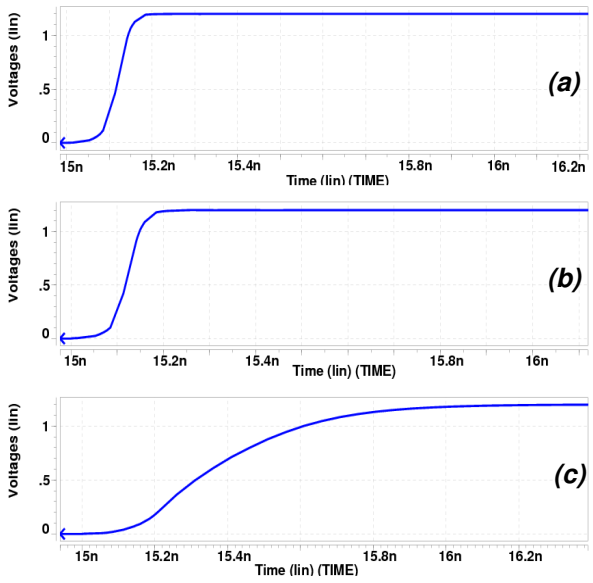

Figure 7. combined write time results for 1 cycle

tor dimensions from the Berkeley standard. For Figure 1, a regular SRAM cell, we used $\lambda = 0.05U$ for 100nm process technology. The length of every transistor in each cell (see Fig. 1, Fig. 5, Fig. 6) is used as 2λ. The width of the transistors goes as follows: all PMOS transistors = 4λ and all NMOS transistors = 6λ.

We begin our capacitance vs write time performance experiments by observing the bit write operation for a value of 1 in a regular SRAM cell. The new value of 1 is written over the the previous value of 0 at 15ns mark as shown in Fig. 7(a). It takes the cell .13 ns to change its state from 0 to 1. The logical bit value corresponds to the voltage probing of a node Q. In the next experiment the same operation was simulated on the SRAM-c model as shown in Fig. 7(c). In the following model we used a 20fF capacitor, the addition of the capacitor results in a write time of 1.14 ns.

The regular SRAM cell write time of .13ns and the SRAM-c cell write time of 1.14 ns represent the lower and the upper bound respectively for the write time of any proposed SRAM model that uses a 20fF capacitor. Any proposed model with similar capacitance parameters must have a write time that falls within those bounds in order to be considered as a viable SEU protection model.

In continuation of the experiments on the write time vs capacitance relationship, we perform a write operation of logical value of 1 in a SRAM-tct cell with a 20fF capacitor, as we have for all other cell models. The new value of 1 is written over the previous value of 0 at 15ns mark as shown in Fig. 7(b). It takes the cell .14 ns to

Cap (fF)	SRAM-c (ns)	SRAM-tct (ns)
0	0.14	0.14
1	0.16	0.14
2.5	0.28	0.14
5	0.4	0.14
10	0.61	0.14
15	0.98	0.14
20	1.2	0.14
25	1.38	0.14
35	2.01	0.14
55	3.43	0.14

Table 1. Capacitance vs write times

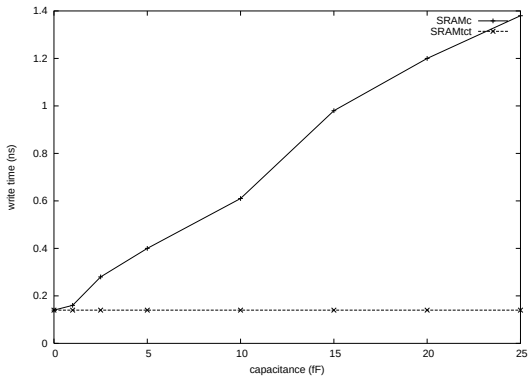

Figure 8. write time of SRAM-tct cell

change its state from 0 to 1. We repeat the following experiments with various values of the capacitor and compare the write times to the SRAM-c and SRAM model shown in Table 1 and graphically depicted in Fig. 8.

It is clear from the Table 1 results, that while the SRAM-c model write time increases with capacitances, the SRAM-tct model write time remains constant, similar to the SRAM model. The constant write time results of SRAM-tct model are attributed to two transistor cell design. During the write process of 0-1 bit value the two CMOS transistors that are connected to the capacitor are in OFF state, refer to Fig. 6. Thus during the write mode as the WL is set to high the SRAM-tct model behaves as the regular SRAM model. During this time the NMOS transistors fed by the WL discharge the capacitor. Then the WL line goes low and the write process is now over the CMOS transistors switch states and the capacitor is re-attached to the design. The re-attachment process of the capacitor will take some energy as the capacitor needs to be charged. The effect of this process is investigated in our next experiment.

For this type of the experiment each of the cell models will experience two write phases, the first write phase will switch the cell value from 0 to 1 and the

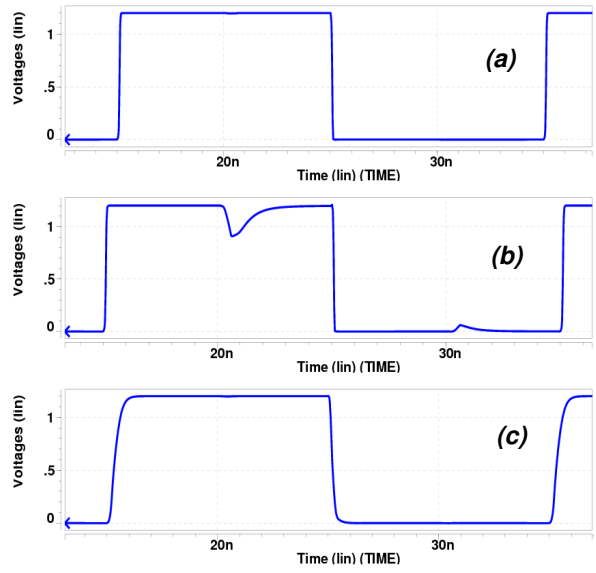

Figure 9. combined write time results for 2 cycles

second write phase will switch the value from 1 to 0. Each of the write phases is set to be exactly 5ns and occur 10ns apart. The experiment is ran on the regular SRAM first, the result can be seen in Fig. 9(a).

The first write phase once again begins at 15ns, it lasts for the next 5ns until 20ns. At this point, the SRAM cell is in standby mode for the next 5ns until at 25ns the second write phase begins. The second write phase changes the value of the cell from 1 to 0. It lasts for the next 5ns until 30ns, the cell is back to standby mode. The exact experiment is run on SRAM-tct and SRAM-c models. The results for SRAM-c are shown in figure 10(c). Its clear that the behavior of the model is similar to the regular SRAM (Fig. 9(a)). with the exception of the write time. The results for SRAM-tct model is shown in Figure 10(b). The results differ from previous two models at 20ns and 30ns mark. These two marks indicate the end of each of the write phases. As we mentioned before the SRAM-tct model disconnects the capacitor and discharges it during a write phase and then re-attaches the capacitor once the write phase is over. The two mentioned marks indicate the affect of the re-attachment of the capacitor to the system. Once the capacitor is re-attached to the system it is not reflective of the potential difference between the node Q and $\bar{Q}$. This potential difference must take some time and energy to adjust on the capacitor. This can be clearly seen at 20 ns. The write phase ends and the capacitor begins to charge up. The potential dips down at this point in time as it takes energy to charge up the capacitor. This is a re-occurring process regardless of the

SRAM-c Cap (fF)	SRAM-c Q_{crit}(fC)	SRAM-tct Q_{crit}(fC)	SRAM-tct Cap Equiv	%
2.5	27.5	30	.5	80
5	31	33.65	3.5	30
10	37.5	43	8	20
20	57	58	17	15

Table 2. Critical Charge vs Capacitance of SRAM-c, SRAM-tct

logical value of node. Granted when a logical value 0 is written to node Q it takes much less energy and time for the capacitor to adjust. The voltage spikes do not change the value of the currently stored.

As mentioned previously the second portion of our experiments simulates SEU upsets in various SRAM models. In the following simulations, a particle strike is modeled by injecting a current pulse at the sensitive node [14]. The pulse has a rather rapid rise time and a gradual fall time. The shape of the pulse can be approximated by the following equation:

$$I(t) = \frac{2Q}{\sqrt{\pi}} \times \sqrt{\frac{t}{T}} \times e^{\frac{-t}{T}}$$

Where Q is the charge collected due to the particle strike and T is the process technology constant. In order to determine Q_{crit} of a cell node, we performed HSpice simulations by injecting current pulses of equation above for various values of Q. The minimum values of Q which results in a cell flip is considered as Qcrit of that node. We produced Q_{crit} values for two SRAM models with variant capacitances. In order to switch the charge from 0 to 1 it requires a lot more energy, thus the cell is more vulnerable to a 1 to 0 flip. Table 2 demonstrates the critical charge for a 1 to 0 flip.

The results from Table 2 show that the tolerance level of the SRAM-tct model is higher then the SRAM-c model. The SRAM-tct model requires less capacitances to achieve the levels of tolerances as the SRAM-c mode. This behavior is associated with the extra addition of the CMOS transistors. We can see that as the capacitances rises the tolerance level difference starts to decrease. The fourth column in Table 1 represents the capacitances equivalent of the SRAM-tct that is required to reach the critical charge of the SRAM-c model in the same row. This shows that we can reduce the capacitance level of the capacitor in the SRAM-tct model while still providing the same level of protection. The fifth column represents the percent reduction

in the capacitance relative to the SRAM-c counterpart. The rapid decline of the percent reduction can be explained by the following. The CMOS transistor's intrinsic strength dominates the critical charge, as the external capacitances of the capacitor increases the transistor has less of the effect. The SRAM-tct design provides write times similar to the regular SRAM cell (Table 1) and also provides greater protection then the SRAM-c model (Table 2).

5 Conclusion

In this paper we first reviewed capacitance based protective models, SRAM-c, SRAM-cc and SRAM-c2. Although these models are effective against SEUs by maintaining the critical charge through extra capacitance. These models penalize the performance of the cells by increase the write time. We addressed the weakness of the write time by introducing a new design, SRAM-tct. We eliminated the influence of the additional capacitance on the write time, while increasing the SEU protection level. Our area overhead is comparable to other memory protection methods and recovery methods reported. Through experimental results we observed that the SRAM-tct model exhibited similar write time behavior as the regular SRAM cell with a minor penalty of 7%.

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