A Novel Radiation Tolerant SRAM Design Based on Synergetic Functional Component Separation for Nanoscale CMOS.

***Abstract*—This paper presents a novel SRAM design for nanoscale CMOS. The new design addresses the problem of low radiation tolerance and high instability for SRAM memories at feature size of 32nm. The novelty of our approach originates from the synergetic functional component separation, where each component serves its unique operational function and has minimal effect on performance of others. The design consists of three different components: the first component is used to store the data, the second one is designed to protect the data at the most vulnerable state and last component serves to extract the data from the SRAM cell. We performed comparative analysis of our design against conventional radiation-tolerant designs in terms of power consumption, level of radiation tolerance, performance, area and stability. The benefits of our new design (high radiation tolerance, high stability, fast performance) were confirmed by extensive simulations in different 32nm technology environments (low power, high performance, bulk).**

I. Introduction

II. Background

A. Classic 6 Transistor SRAM cell

The classical design for SRAM memory is a six transistor design, $6T$, shown in Fig. 1. The $6T$ cell uses the positive feedback between two cross coupled inverters formed by transistors: $N1 - N2$ (pull-down) and $P3 - P4$ (pull-up) to store one bit of data. The data in the $6T$ cell is accessed (read mode) and deposited (write mode) through the bit-lines, BL and $\overline{BL}$ by activating WL. The access transistors ($M5$ and $M6$) isolates the cell from other circuitry during standby mode. The cell design must satisfy two different conditions in order to have optimal readability and fast writability: $W_{PD} > W_{PG}$ and $W_{PG} > W_{PU}$, where W_{PD}, W_{PG}, W_{PU} are the width of pull-down, pass-gate (access) and pull-up transistors respectively.

Stability and robustness of an SRAM cell is characterized by its ability to retain stored data. Stability of SRAM during read mode is usually quantified by the metric static noise margin (SNM) as the maximum DC voltage required to flip the stored value. [2], [3]

The cell components responsible for cell stability and performance, $N1 - N2$, $P3 - P4$, $M5 - M6$, perform dual function to read/write the data, $blue$ and red region in Fig. 1. The conjoined functionality makes it rather difficult to attain optimal design in terms of either fastest write performance or highest stability.

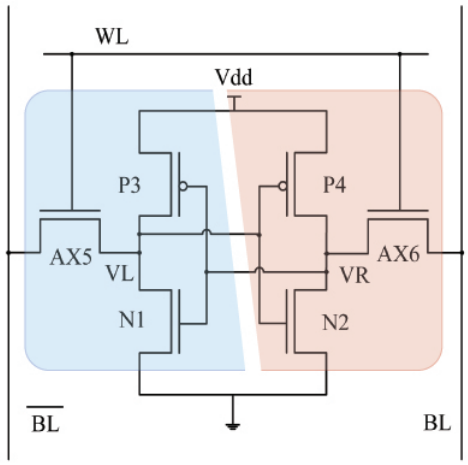

Fig. 1. Classical 6 Transistor SRAM Design

B. Eight Transistor SRAM cell

There are a few alternative designs to $6T$ memory cell that address the issue of dual functionality of the $6T$ cell and its drawbacks. [**?**], [**?**], [**?**]. The most common design consists of eight transistor SRAM cell, $8T$, shown in Fig. 2. The $8T$ cell uses the same type of design to write the data to the cell as the $6T$ cell, the $blue$ region in Fig. 2. However, in order to read the data a new component is added to the $6T$ cell, a separate read port. The read port, red region in Fig. 2, consists off transistors $R7$ and $R8$, a read word line, RWL and a read bit line, RBL.

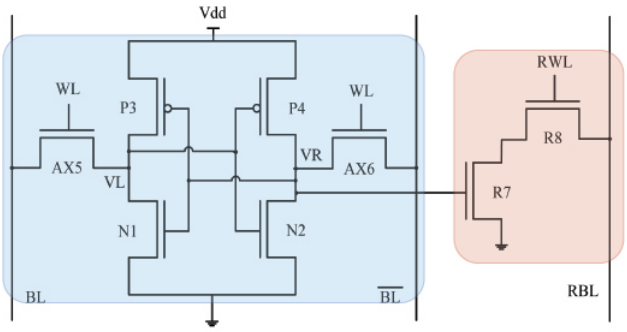

Fig. 2. 8 Transistor SRAM Design

Such functional component separation provides a more

optimal design in terms of read and write functionality. The write constraints of $W_{PD} > W_{PG}$ only apply to the access transistors and the inverters while the $W_{PG} > W_{PU}$ condition is completely relaxed due to the addition of the read port. Therefore, the width dimensions of the inverters can be scaled down to produce a much more optimal memory cell. However, there are disadvantages to this design. The addition of the read component to the cell does increase the overall area of the cell. The dimension scaling of the storage inverters does decrease the overall soft error tolerance compared to the $6T$ design.

C. Soft Errors

A Single Event Upset (SEU) in the SRAM occurs when a charged particle strikes a sensitive node and flips the state of the SRAM cell from 0 to 1, and vice versa, causing a soft error. This does not damage the device permanently and the data can be re-written if the error is detected. But, in complex systems the correction is highly unlikely and this data error can eventually lead to system failure. The reverse-biased junctions, created by the drain and substrate of the OFF-transistors, of the cell are most sensitive nodes to the particle strike. These charged particles can originate directly from radioactive materials and cosmic rays or indirectly as a result of high-energy particle interaction with the semiconductor itself.

Immediately after a particle strike, the generated electron-hole pairs are collected at the opposite voltage terminals of the reverse-biased junction and thus causing a current pulse with width of few hundred pico-seconds. The memory cell flips when the collected charge, Q, is larger than the stored charge at the struck node. The minimum charge required to flip the bit stored in the cell is called Q_{crit}. The Q_{crit} not only depends on the collected charge but also on the shape of the current pulse [**?**], [**?**], [**?**], [**?**], [**?**], as well as the strength of the gate driving the node. A 1 to 0 flip occurs when a particle strike discharges the charge stored at the drain of the OFF-NMOS transistor, and similarly, a 0 to 1 flip occurs when a particle strikes at the drain of the OFF-PMOS transistor. As technology scales down, the charge stored at the sensitive nodes of the memory cell is reduced because $Q_{node} = C_{node} \times V_{dd}$ making SRAM more prone to soft errors.

D. Soft Error Protection Methods

There have been many solutions to reduce the sensitivity of SRAM cells to soft errors, ranging from hardening the existing transistor sizes to the addition of extra components in the cell design to protect the cells. The main focus of all these solutions is to preserve the charge stored in the system.

Capacitive-based SEU protection models, shown in Fig. 3 conventionally use a charge buffer, a capacitor or multiple capacitors, between the nodes $V1$ and $V2$. These capacitors keep the potential of the nodes remaining the same even if a SEU happens at one of these nodes and thus the cell state is not affected. The additional capacitance increase the soft error tolerance of the cell. But, the large area overhead due to these extra capacitor is a problem. One model to address the area problem was pioneered in [**?**], $SRAM$-C, with the capacitors vertically stacked above the SRAM cells, to minimize the footprint. The major weakness of capacitor-based models is the fact that they increases the write time required to change the state of the cell.

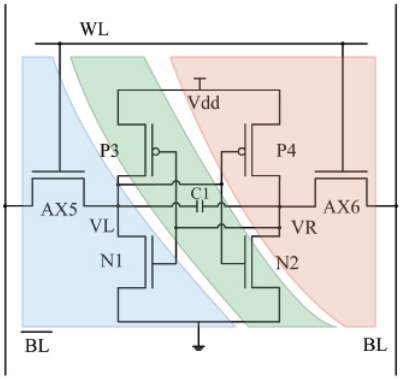

Fig. 3. Capacitor based SRAM Design

In standard harding the physical characteristics of the transistors are increased (the width and the length of the transistor) in order to increase the tolerance level of the cell itself. The drawbacks to this method in terms power consumption are attributed to the increase of the physical aspects of the SRAM cell transistors.

The common theme in all of these protection techniques is the added functionality of protecting the data stored to the existing components through either modification of the components or minor additions. The merger in functionality results in adverse effects on the characteristic of the SRAM cell in terms of power consumption, performance, stability and area.

In our previous work, we proposed a design that attempted to separate the soft error protection circuitry from the storage cell. In this $SRAM - TCT$ design, additional two $CMOS$ transistors along with two $NMOS$ transistors and a vertically stacked capacitor are connected to the storage nodes, as shown in Fig. 8 by the $green$ region. The $CMOS$ transistors act as a switch and are activated only during the standby mode through $\overline{WL}$. The capacitor act as a charge buffer and improves the overall soft error tolerance of the cell. During a read or write mode the $NMOS$ transistors are turned ON and capacitor discharges through it. Once the SRAM cell goes back to the standby mode (data hold) the capacitor is re-introduced into the system [**?**].

In TCT design, the actual storage cell still uses the classical six transistor approach of merged functionality for the inverters as seen by the red and blue boxes in Fig. 8. Therefore, the TCT design is unable to be fully optimized in terms of optimal stability and performance.

III. Synergetic Component Separation Memory

We propose a novel design, $SRAM$-SCS, that uses synergetic component separation in order to address soft error

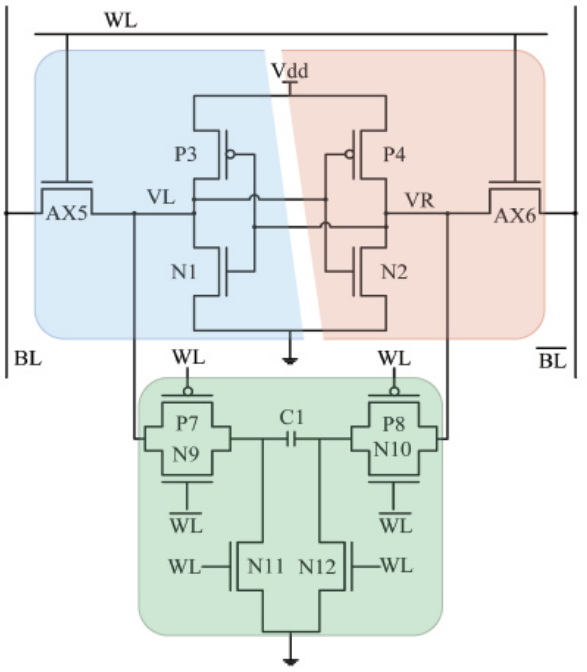

Fig. 4. SRAM-TCT design with separated protection circuit

stacking technique shown in **??**. Furthermore, we believe that compared to the existing protection methods the SCS design will provide vast advantages in performance, radiation tolerance and overall cell stability.

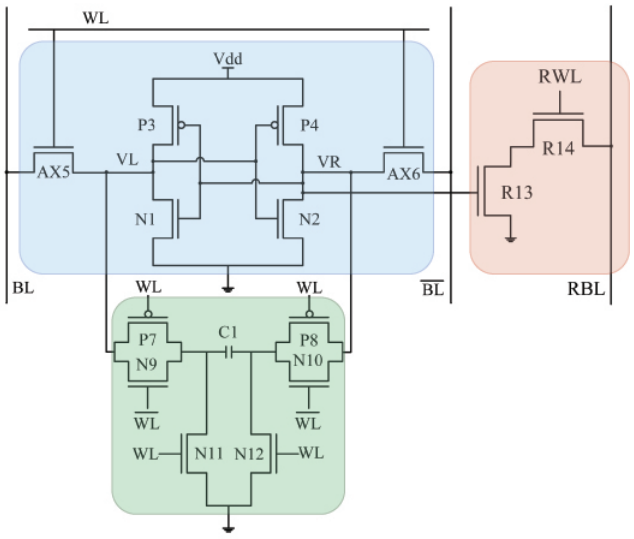

Fig. 5. SRAM-SCS design with full component separation

protection while optimizing data storage and retrieval functionality. The SCS design is shown in Fig 5: the $blue$ region represents the components responsible for writing and storing the data, the red region represents the components responsible for reading the stored data, and the $green$ region represents the components that are used to increase the soft error tolerance of the stored data. The full component separation results in optimization in each functional region.

The dimension of the write / store component, $blue$ region is governed by only $W_{PG} > W_{PU}$ constraint, where W_{PG}represents the width of the $AX5$ and $AX6$ transistors and W_{PU} represents the width of the $P3$ and $P4$ transistors in Fig. 5 The read component, red region, uses a read port design from 8T SRAM cell. The $R13$ and $R14$ transistors are used to retrieve the data from the inverters by the RWL and RBL.

The on-demand protection component of the design, $green$ region, uses a vertically stacked capacitor $C1$ to create a charge buffer between the data nodes, VL and VR. The overall capacitance of the cell during the data retention mode (stand-by mode) is increased, therefore the overall level of soft error tolerance is increased as well. The $C1$ capacitor is kept separate from the storage cell during write operations by the two CMOS gates, $P7/N9$ and $P8/N10$, through the additional word line, $\overline{WL}$. Also during the write operation, the $C1$ capacitor is discharged by the $N11$ and $N12$ transistors. Thus the $C1$ capacitor can reflect the new value stored in the cell without affecting the time it takes to store the new value.

The overall component separation does have disadvantages in terms of area and power consumptions. We partially address the additional area foot print by using the vertical capacitor

IV. Simulation and Results

In our simulations, we isolate the effects of functional component separation for unprotected designs (read and write functionality) and for protected designs (read, write and protect functionality) on performance, power consumption, area, leakage, radiation tolerance and stability. We focus on two different applications (low power and high performance) for a single 32nm technology node.

As we mentioned earlier, the classic example of functional component separation for standard design is a 8 transistor, $8T$, cell (separate read port and separate write component) compared to a 6 transistor cell that has no functional separation (cell must satisfy both read and write optimal conditions). We construct the two models for unprotected designs, $6T$ and $8T$ cells with the following specifications: for minimum transistor length we use, $L_{min} = 2\lambda$, the transistor width depends on the transistor and its function. The overall width dimensions are shown in Table I. The Table **??** uses the transistor labeling shown in Fig. 1 and Fig. 2. We use the pull-down transistor ($N1$, $N2$) to the access transistor ($AX5$, $AX6$) ratio, $\beta = 2$, and the access transistor ($AX5$, $AX6$) to pull-up transistor ($P3$, $P4$) ratio,$\gamma = 2$, for 6T cell. For 8T cell, we use $\beta = 1$ and $\gamma = 1.5$.

For protected designs we investigate designs without any functional separation, partial separation and our proposed design with synergetic functional component separation. We construct five models: two hardened designs of the 6 transistor cell, the vertically stacked capacitor solution $SRAM\text{-}C$, our previous $SRAM\text{-}TCT$ design and our new $SRAM\text{-}SCS$ design. For all protected designs we use the minimal transistor length, $L_{min} = 2\lambda$.

Transistor Widths for unprotected designs

Design	N1,N2	P3, P4	M5, M6	M13, M14
6T	16λ	4λ	8λ	-
8T	6λ	4λ	6λ	6λ

TABLE I
WIDTHS OF TRANSISTORS FOR 6T AND 8T DESIGNS SHOWN IN FIG. 1 AND FIG. 2

For the hardened designs, $6TH2X$ and $6TH4X$, we harden the transistors by increase the width of all transistors by 2 or 4 times the width of the classical 6 transistor cell. All the width dimensions for the protected designs are shown in Table II using the transistor labeling from Fig. 1 and Fig. 5.

Transistor Widths for protected designs

Design	N1,N2	P3, P4	M5, M6	M7-M12	M13, M14
6T2X	32λ	8λ	16λ	-	-
6T4X	64λ	16λ	32λ	-	-
SRAM-C	16λ	4λ	8λ	-	-
TCT	16λ	4λ	8λ	6λ	-
SCS	6λ	4λ	6λ	6λ	6λ

TABLE II
WIDTHS OF TRANSISTORS FOR 6T HARDENED (2X, 4X) SRAM-C, TCT AND SCS DESIGNS

All the designs are constructed in Hspice and Nanosim. We test the characteristics of the designs in two different applications (low power and high performance) for $32nm$ process technology obtained from Berkley Predictive Technology Model (BPTM) data [**?**]. We use the nominal operation voltage: $1.0V$ for low power application and $0.9V$ for high performance application. To effectively analyze the advantages and disadvantages of component separation for radiation tolerant designs we compare the results of our simulations between the non protected designs and protect designs.

A. Area

We used a thin layout topology to layout the seven designs in 90nm logic library. We estimated the area of the designs in 32nm technology by extrapolating the results for the technology node. The data was then normalized to the $6T$ cell foot print, $.195\mu m^2$, and can be seen in Table III.

Normalized Area

Design	6T	8T	6TH2X	6TH4X	SRAM-C	TCT	SCS
Area	-	30%	88%	266%	5%	61%	86%

TABLE III
AREA NORMALIZED TO A 6T CELL WITH THE AREA OF $.195\mu m^2$

The $8T$ cell is only 30% larger than the $6T$ cell due to overall transistor scaling down. The harden designs, $6TH2X$ and $6TH4X$, occupy expected area compared to the $6T$. The $SRAM\text{-}C$ design occupies only additional 5% of area due to the vertical stacking of the capacitors used in the design. The TCT design requires 61% additional area for the protection circuit. The SCS design requires a bit more area compared to TCT design for the additional read port. The overall area increases by the TCT and SCS designs are still less then the hardening designs.

WriteTime Performance

Design	Bulk $V_{dd} = 1.0V$	High Performance $V_{dd} = 0.9V$	Low Power $V_{dd} = 1.0V$
$6T$	$16.8ps$	$27.0ps$	$66.5ps$
$8T$	$11.4ps$	$15.7ps$	$45.6ps$
$6TH2X$	$16.2ps$	$24.1ps$	$63.1ps$
$6TH4X$	$15.6ps$	$22.8ps$	$58.5ps$
$SRAM\text{-}C$	$82.6ps$	$115.0ps$	$337.0ps$
TCT	$18.9ps$	$32.7ps$	$70.6ps$
SCS	$15.3ps$	$20.0ps$	$58.0ps$

TABLE IV
PERFORMANCE NEED CAPTION

B. Performance

We used the $10-90\%$ voltage rule to accurately determine the time it takes for the SRAM cell to change states. We focus on the node that goes through the low to high state change as this is the longest write time delay of the two simultaneous state changes happening during a write operation. The observed write time delay corresponds only to a single bit cell for all the simulated designs without any capacitive load. For a large column of SRAM cells these values will differ, however the relationship between the designs will remain the same. The write delay data for each design is compiled in Table 7 ordered by the technology node.

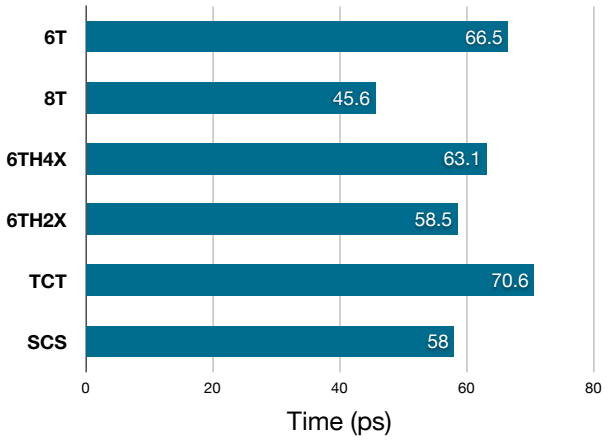

Fig. 6. 6 Transistor SRAM Classical Design

From Table 7 it can be seen that the high performance 32nm technology library increases the overall performance of all

the designs, even under lower nominal operating voltage. It is also clear that the SRAM-C design is the slowest design compared to all the others, such observation is consisted between different technology nodes. In order to focus on the relationship between the designs in terms of performance, we excluded the SRAM-C design and graphed the data in Fig. 7

The $8T$ design is the fastest design compared to $6T$ and all the protection designs, increasing the performance by 33%. The benefits of functional component separation is clearly demonstrated here, as the write function component is optimized for fastest performance and delivers such performance. The hardening of the $6T$ design improves its performance as the transistor strength increases with each hardening step, however the constraints of the read component propagate through each hardening step. The TCT design is slower then the classical $6T$ cell by 6%. Compared to the hardened designs, $2x$ and $4x$, the TCT cell is slower by 11.8% and 20.7% respectfully. The advantages of component separation seen in $8T$ cell design is also seen in SCS design as well. The SCS design is faster then all other protection designs that were tested.

C. Soft Error Tolerance

To determine the soft error tolerance of each design, we simulated an SEU upset for each case through an injection of current pulse at a sensitive node of the cell [**?**]. The current pulse has a rather rapid rise time and a gradual fall time and provides a similar effect to an actual particle strike. The shape of the pulse can be approximated by the following equation:

$$I(t) = \frac{2}{\sqrt{\pi}}\frac{Q}{T} \times \sqrt{\frac{t}{T}} \times e^{\frac{-t}{T}}$$

Where Q is the charge collected due to the particle strike and T is the time constant for the charge collection process and is a property of the CMOS process used for the device.

The minimum values of Q which results in a cell flip is considered as Q_{crit} of that cell node. We produced Q_{crit} values for all designs for both low power 32nm and high performance 32nm technologies. We use the critical charge value, Q_{crit}, for a 1 to 0 flip as a reliability parameter. A higher value of Q_{crit} results in higher level of soft error tolerance for a specific design. For capacitor based solutions we investigated capacitor values between $3ff - 10ff$, however for comparison purposes we used the minimum value of $3ff$ for $SRAM\text{-}C$, TCT and SCS designs. We compile the data in Table V.

From Table V, we can see that the $6T$SRAM design has 25% higher tolerance level then the $8T$ cell for low power 32nm technology. For high power technology, $6T$ cell provides 10% higher protection. The reduction in transistor sizing for the $8T$ cell results in lower overall cell capacitance, which translates into lower critical charge. The protection designs: $6TH2X$, $6TH4X$, $SRAM\text{-}C$, TCT, SCS, all provide higher levels of protection compared to $6T$ or $8T$ cells. For the designs with capacitor based solution, the tolerance level is very similar and falls between the $6TH2X$ and $6TH4X$ solutions for low power technology. However, for high performance application with much stronger transistor characteristics the hardening designs: $6TH2X$ and $6TH4X$ provide higher level of soft error tolerance.

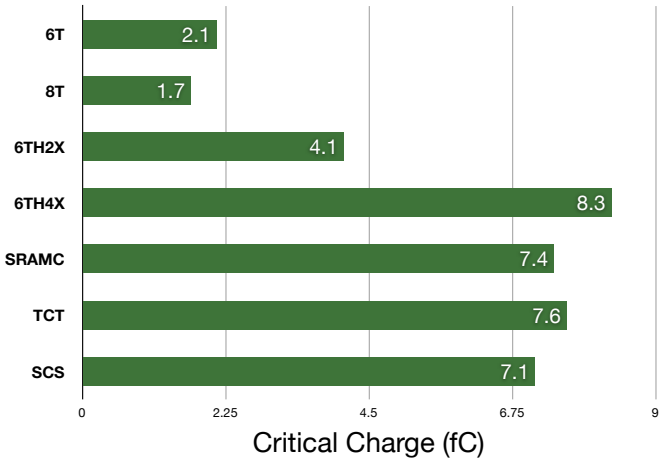

Fig. 7. 6 Transistor SRAM Classical Design

Soft Error Tolerance for 32nm

Design	Bulk $V_{dd} = 1.0V$	High Performance $V_{dd} = 0.9V$	Low Power $V_{dd} = 1.0V$
$6T$	$3.8fC$	$3.6fC$	$2.1fC$
$8T$	$3.5fC$	$3.3fC$	$1.7fC$
$6TH2X$	$8.5fC$	7.7 fC	$4.1fC$
$6TH4X$	$17.7fC$	$15.7fC$	$8.3fC$
$SRAM\text{-}C$	$6.7fC$	$7.0fC$	$7.4fC$
TCT	$7.3fC$	$7.4fC$	$7.6fC$
SCS	$7.1fC$	$7.2fC$	$7.1fC$

TABLE V
CRITICAL CHARGE NEED CAPTION

D. Power Consumption

For power, we used the peak power measurements during a write operation of a single bit cell for all the tested designs. The data is shown in Fig. VI.

For all technology nodes, the unprotected $8T$ design consumes less power then $6T$ design. The power consumption savings are produced by the smaller transistors of the $8T$ design. The savings in power heavily depend on the actual technology node used. For the protected designs, the SCS design consumes less power than any other design. The savings in power are achieved through the transistor sizing reductions. The power consumed by the additional circuitry required to protect the data and read the data in the SCS design still provide the overall savings when compared to other protective designs.

Power Consumption

Design	Bulk $V_{dd} = 1.0V$	High Performance $V_{dd} = 0.9V$	Low Power $V_{dd} = 1.0V$
$6T$	$.172mW$	$.166mW$	$.119mW$
$8T$	$.096mW$	$.109mW$	$.111mW$
$6TH2X$	$.317mW$	$.316mW$	$.223mW$
$6TH4X$	$.707mW$	$.684mW$	$.448mW$
$SRAM\text{-}C$	$.490mW$	$.269mW$	$.183mW$
TCT	$.544mW$	$.273mW$	$.259mW$
SCS	$.218mW$	$.241mW$	$.168mW$

TABLE VI
POWER CONSUMPTION NEED CAPTION

E. Static Noise Margin

We used Seevinck's method [] to estimate the static noise margins (SNM) of the SRAM cells. The voltage transfer characteristics of the inverters are generated for the read accessed SRAM cells to find the worst-case SNM for the cells. The side of the maximum embedded square between the lobes of the generated curve, called the 'butterfly curve', represents the immunity to static noise, SNM. Figure **??** shows the butterfly curves generated for SRAM cells . Table **??** shows the SNM of SRAM cells during a read access.

SNM

Design	Bulk $V_{dd} = 1.0V$	High Performance $V_{dd} = 0.9V$	Low Power $V_{dd} = 1.0V$
$6T$	$58.4mV$	$107.4mV$	$205.9mV$
$8T$	$260.9mV$	$279.2mV$	$401.6mV$
$6TH2X$	$59.7mV$	$108.0mV$	$206.2mV$
$6TH4X$	$61.0mV$	$108.2mV$	$206.4mV$
$SRAM - C$	$58.4mV$	$0.1074mV$	$205.9mV$
TCT	$58.3mV$	$107.4mV$	$205.9mV$
SCS	$260.4mV$	$279.1mV$	$401.6mV$

TABLE VII
SNM NEED CAPTION

We can see that the $6T$ has the least static noise robustness while the $8T$ has superior SNM for all the technology application nodes. This is attributed to the separate read port of $8T$ cell where the data is read out without disturbing the node potential. For $6T$, the rise in node potential during the read operation shifts the voltage transfer characteristics resulting in a lesser SNM. The increase in SNM from bulk to high performance technology node for the same cell is the result of the improved transistor strength. The $6TH2X$, $SRAM\text{-}C$ and TCT cells also shows the same SNM levels due to the fact that the SNM depends only on the transistor length and transistor sizing ratio not on the absolute transistor widths. We can also see that the SCS cell has maximum SNM levels for the application node because of the separate read port.

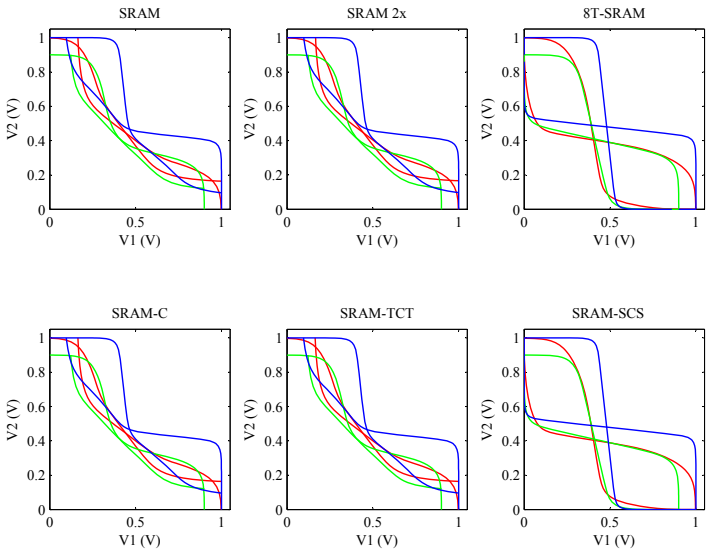

Fig. 8. Capacitor based SRAM Design

V. CONCLUSION

In this paper, we proposed a novel radiation tolerant SRAM design, $SRAM\text{-}SCS$. The SCS design is based on synergetic functional component separation. Each component of the design is responsible for its unique function: writing the data, reading the data and protecting the data from soft errors. We compared the new design with other soft error protection methods as well as classical 6 and 8 transistor SRAM designs. The SCS design, compared to other protection designs, provides excellent soft error protection, consumes the least amount of power and produced fastest performance. The SCS design also provides the most stable and robust cell design.

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